Large Scale Integrated (LSI) Bipolar Circuits,

A study of Integrated Injection Logic.

by

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in candidature for the degree of Doctor of Philosophy.

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DECLARATION

I declare that except where stated, the work contained in this thesis is original and has not beem submitted for any other degree.

Signed.....Les. W. Kennedy....

Les. W. Kennedy

Supervisor.....M. McPherson...

SUMMARY

This thesis is a description of integrated injection logic, a bipolar large scale integration technique.

Various alternatives to integrated injection logic are discussed and the advantages and disadvantages of each are outlined. The integrated injection logic structure is introduced and its advantages over other solutions are described.

Those device characteristics necessary for successful operation of the integrated injection logic gate are established, and the physical mechanisms controlling D.C. and A.C. performance are investigated theoretically. These theoretical investigations are compared with experimental observations.

The behaviour of the I^2L gate is shown to be very dependent on the characteristics of the epitaxial emitter and the intrinsic base region of the device. In an extension to the basic device theory it is shown that the device characteristics can be related to the transistor characteristics in the conventional mode of operation.

As the technique is primarily for large scale integration a considerable effort has been placed on yield studies. These yield studies have included work on the following: parametric control, photoengraving and silicon crystallographic defects.

Silicon crystallographic defects are shown to be a major yield hazard and appropriate actions to eliminate them as failure mechanisms are described.

ACKNOWLEDGEMENTS

Although the author has produced a large number of the devices and samples investigated in this thesis, he is indebted to the staff of The Plessey Company's Allen Clark Research Centre for their assistance in producing I^2L integrated circuits.

The X-ray topographs and transmission electron micro photographs presented in this thesis have been prepared for the author by Dr.R.Ogden and Mr.P.Augustus of The Allen Clark Research Centre.

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CONTENTS

CHAPTER 3 COMPREHENSIVE INJECTION MODEL OF THE I^2L GATE

LIST OF SYMBOLS

A	junction area as defined in text.
C(O)	junction capacitance at OV.
D_n	diffusion coefficient in p-type material
D	diffusion coefficient, low doped epitax
D^+	diffusion coefficient, in Buried N^+
E_g	silicon energy gap
ΔE_g	energy gap narrowing due to heavy doping
E	electric field
F_{GC}	correction factor for 2-dimensional nature of injector transistor
I	currents as defined
J_{NC}	current density of carriers injected into contact covered regions of the I^2L gate
J_{NO}	current density of carriers injected in oxide covered regions of the base of the I^2L gate
J_{PO}	current density of carriers injected into the epitax/buried N^+ of the I^2L gate
J_{NI}	current density of carriers injected in the intrinsic base region of the I^2L gate (collector current density)
J_{PL}	lateral re-injection current per unit length of the I^2L gate.
k	boltzmann's Constant
L	length of lateral pnp injector
L_E	diffusion length in the epitax
L^+	diffusion length in the buried N^+
L_n	diffusion length in p-type material
M	avalanche multiplication factor
N	doping density

N_D	donor concentration
$N_{D_{EPI}}$	donor concentration in epitax
N^+	donor concentration in buried N^+
N_A	acceptor concentration
p	hole concentration
p_o	hole concentration at depletion boundary in epitax
p_1	hole concentration at epitax buried N^+ boundary
n	electron concentration, also various factors as defined in text.
n_o	electron concentration at depletion boundary in the base
n_s	electron concentration in base at oxide boundary
n_i	intrinsic carrier concentration
n_{ie}	effective intrinsic carrier concentration
n_p	electron concentration in p-type material
n_n	electron concentration in n-type material
p_n	hole concentration in n-type material
p_p	hole concentration in p-type material
q	electronic charge
Q	stored charge
S_o	surface recombination velocity
T	absolute temperature
t_{de}	extrinsic delay
t_{di}	intrinsic delay
t_s	storage time
t_r	rise time

τ_S	storage time constant
τ_C	collector time constant
τ_B	base time constant
τ_E	emitter time constant
τ	epitax minority carrier lifetime
τ^+	buried N^+ minority carrier lifetime
τ_n	minority carrier lifetime in base
x_j	junction depth
W_b	base width
W^+	width of buried N^+
α	common base current gain (see text)
β	common emitter current gain (see text)
ψ	potential across epitax buried N^+ boundary
V	voltage
ϵ_S	dielectric constant of silicon
ϵ_o	dielectric constant of free space
ϵ_r	relative dielectric constant
$\mathcal{E}$	electric field in region under reverse bias
ω_T	angular cut-off frequency
BV_{CBO}	collector-base breakdown voltage
BV_{CEO}	collector-emitter breakdown voltage
V_{pt}	punch through voltage
I_{CBO}	collector-base leakage current with emitter open circuit
I_{CEO}	collector-emitter leakage current with base open circuit

V_{APP}	applied forward voltage to a p-n junction
V_{be}	emitter base forward bias
C	capacitance
I_{BO}	base saturation current

Certain symbols are defined in the text because of multi-use.

Note on Experimental Graphical Results

In general, experimental points are not included on experimental curves except where results are difficult to duplicate or are contentious. Large numbers of the curves are copies of results made with chart recorders and are thus continuous experimental points. Results not from chart recorders in which data points are not included are easy to reproduce and no data points lie significantly away from the drawn line.

GENERAL INTRODUCTION

Integrated Injection Logic (I^2L) was announced at the 1972 IEEE International Solid State Circuits Conference in Philadelphia. This initial announcement resulted in a large amount of activity and experimentation amongst the major bipolar integrated circuit manufacturers who saw I^2L as an opportunity for them to encroach on the market previously dominated by the MOS integrated circuit manufacturers, i.e. large scale integration of digital functions. I^2L logic can be produced directly on a simplified bipolar process or on a standard process to improve the product capability of that process.

The major part of the work carried out in this thesis has employed a state of the art high performance shallow diffused bipolar process not previously intended for large scale integration. In order to establish the validity of the theoretical and experimental conclusions, I^2L on an older, deeper diffused process was also investigated.

The theoretical treatments used in some cases are extensions to treatments published by other authors, for example, the Ebers-Moll treatment of the I^2L gate in Chapter 2; this approach is due to Weidmann and Berger but the results described are obtained from the current work.

The thesis consists of two parts: Chapters 1 to 6 deal with the operation of the I^2L gates and Chapter 7 with

yield of I^2L gates. Because of this diversity, the references for Chapter 7 have been listed separately from those for Chapters 1 - 6 and the Appendices.

As each new subject is introduced a brief description of relevant contemporary literature is given, with suitable references. It is assumed throughout that the reader has some basic knowledge of both silicon integrated circuit technology and bipolar device physics. The reader is referred to the following texts for basic processing and device details:

Physics and Technology of Semiconductors

A.S. Grove Wiley

Transistor Engineering

A. Phillips McGraw Hill

CHAPTER 1

LARGE SCALE INTEGRATED (LSI) BIPOLAR CIRCUITS

1.1. INTRODUCTION

Integrated Injection Logic, I^2L, is a recent addition to the LSI circuit designer's tools. It is a technique which offers significant advantages over other bipolar approaches. In order to grasp the importance of I^2L it is necessary to discuss some elementary relationships concerning LSI circuits, in particular the role of bipolar technologies in LSI circuit design.

The increasing demands of the electronics industry has produced requirements for larger and more complex integrated circuits. These large scale integrated circuits have been produced using various technologies; however, P-channel MOS techniques were the first processes to reach the maturity required to produce very complex functions. N-channel MOS technology is now available which has significant speed advantages over P-channel devices.

The requirements of an LSI technology are:-

(1) The process should be easily producible thus giving high yield and low unit cost.

(2) Power consumption should be small per logic function, thus minimizing chip dissipation.

(3) The figure of merit known as power-delay product should be small, giving high speed operation at low power consumption.

(4) High packing density is required.

Although there are certainly other requirements the above are of paramount importance, and justify the dominance of MOS techniques in the manufacture of LSI circuits.

P-MOS technologies generally require two depositions, three oxidations, four photoengravings and no epitaxial layer. Depletion load N-MOS processes are only slightly more complex. This results in MOS LSI circuits being outstandingly producible (1,2,3)

Planar epitaxial bipolar technologies need at least four depositions, six oxidations, six photoengravings and an epitaxial layer for the simplest of processes. As each process operation reduces yield it is apparent why bipolar technologies have been slower than MOS in achieving LSI status. Also MOS devices, being self isolating, have a packing density advantage over conventional planar bipolars where some of the silicon surface is consumed by some form of isolation channel.

A number of elegant techniques have been developed to produce bipolar LSI circuits. The TRW Company have developed the Triple Diffused ('3-D') process which sacrifices transistor performance in order to produce a simple bipolar technology not requiring epitax (4,5,6). Murphy and Glinski (7) proposed the Collector Diffused Isolation (CDI) structure which the Ferranti Company are now developing to maturity as a bipolar LSI technique. Although CDI maintains fairly good transistor parameters whilst achieving high packing density and practicable devices, breakdown voltages are low ($BV_{CEO} \sim$ 8V) and frequency response is inferior to that of dedicated high speed bipolar processes ($f_T \sim$ 1 GHz). This is inherent in the epitaxial base structure of the devices. The Fairchild Company have developed the Isoplanar technique to a state where large bipolar circuits are producible.

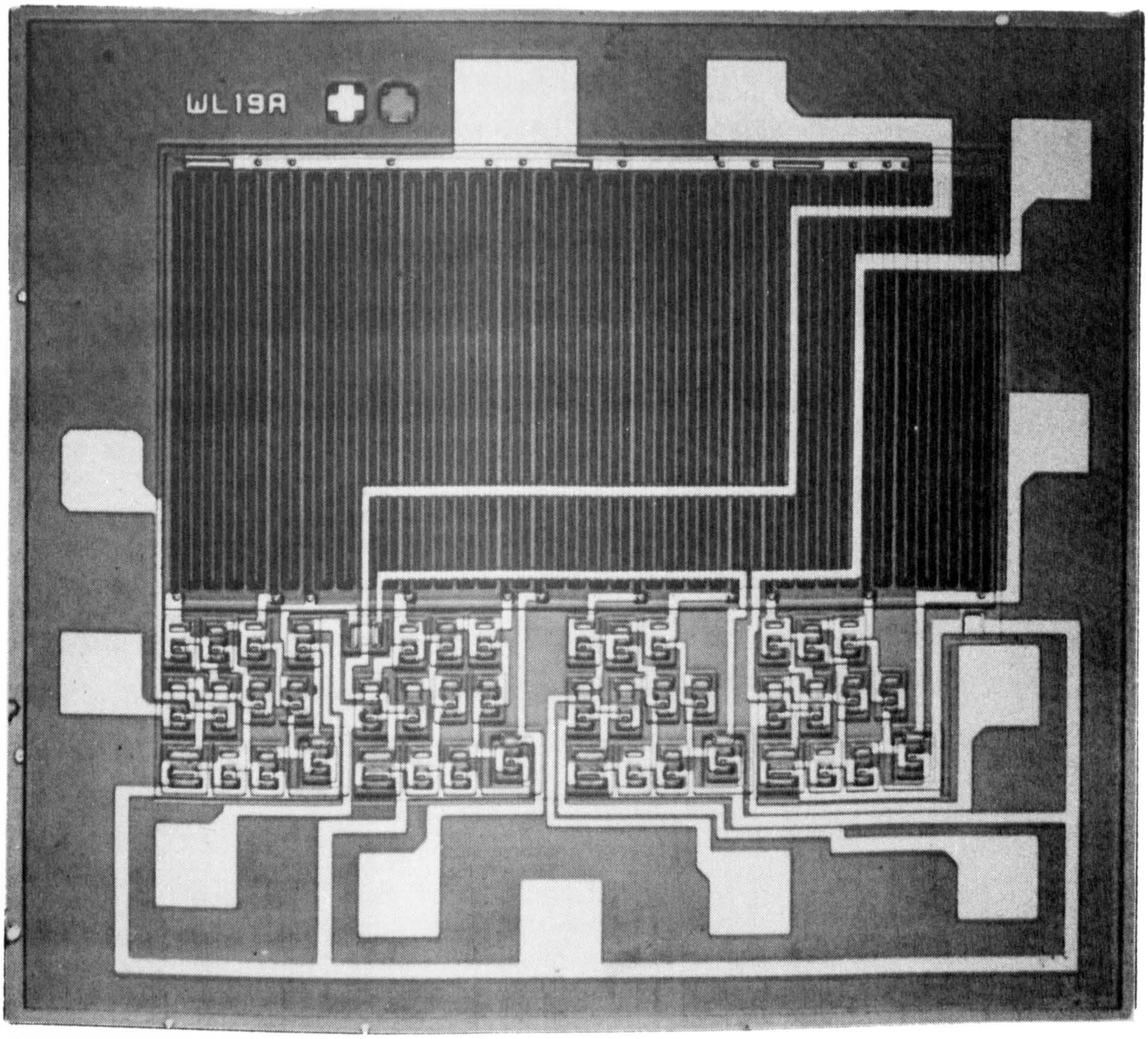


FIGURE 1.1 LOW POWER INTEGRATED CIRCUIT CONTAINING FOUR MONOSTABLE FUNCTIONS

Although processing techniques are technologically difficult, Fairchild have solved them. Unfortunately apart from the basic device structure (8), little has been published on Isoplanar technology.

It is mandatory that LSI circuits are operated at 'low power' per logic block. This is in order to minimise total power dissipation. Low power is achieved by limiting current consumption, in which case the area occupied by the large resistors required can become intolerable. Figure 1.1. shows a Plessey IC containing four low power monostable functions. The area occupied by resistors (2MΩ total) is approximately twice that of the active elements. Large resistors can limit switching speed by producing large RC time constants. If LSI bipolar circuits are to be produced a means of defining low currents must be satisfactorily found.

Integrated injection logic I^2L (also known as Merged Transistor Logic MTL)satisfies the requirements for bipolar LSI. It is a technique which provides high packing density self-isolating devices with a low power delay product and it can be fabricated with a four mask process. The technique originates from the Philips and IBM Companies in 1971 (9.10). Seven mask processing allows products to be fabricated consisting of both I^2L circuits and conventional circuitry.

1.1.1. Triple Diffused ('3D') Bipolar LSI

Bipolar IC processes are more complex but have a higher performance than their MOS counterparts. One approach to bipolar LSI is to simplify processing and sacrifice performance.

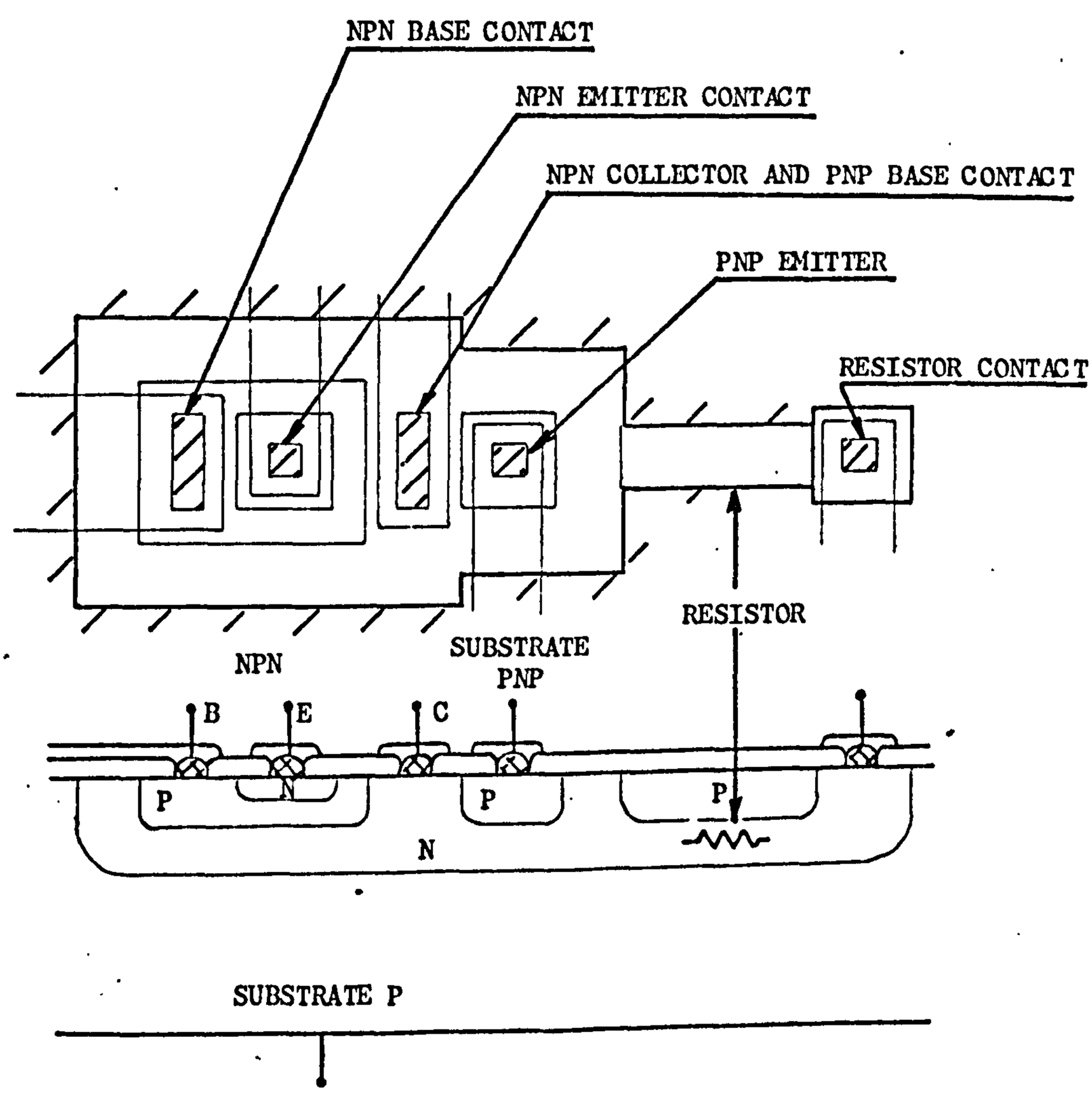


Figure 1.2

TYPICAL TRIPLE DIFFUSED STRUCTURE

"3D"

This is the 3D approach.

Figure 1.2. shows a plan and cross section of a 3D structure. The n-p-n transistors are fabricated on a lightly doped P-type substrate. The processing sequence is as follows. A deep diffused phosphorus region forms the collector; the base and emitter are formed inside this region in the normal way. The transistors so fabricated are self isolating with the collector phosphorus diffusion defining the isolation junction. The npn transistors have a very high collector series resistance (125Ω typical); common collector substrate pnp transistors are available. Using a derivative of emitter coupled logic called emitter function logic, the TRW Company have fabricated some of the largest bipolar IC's known (4,5,6,). Power delay* products of 10 picojoules are claimed with a 30 MHz shift register capability. '3D' avoids epitaxy (which is shown later to be a significant yield hazard), and requires only five photoengraving operations. The disadvantages of '3D' are:-

(1) Analogue functions are difficult to implement.

(2) The inherent transistor structure of the 3D process offers little improvement in speed of operation over performances already achieved.

(3) The npn transistor performance is severely degraded.

(4) No isolated pnp transistor is available.

1.1.2. Collector Diffused Isolation.

Collector Diffused Isolation is a simple epitaxial IC technique. The basic npn device structure is shown in Figure 1.3. The device is fabricated as follows. A buried N^+ pattern is diffused into a p-type substrate and a p-type

* Power delay product is the power consumed by a logic gate multiplied by the gate delay of that gate at that operating power.

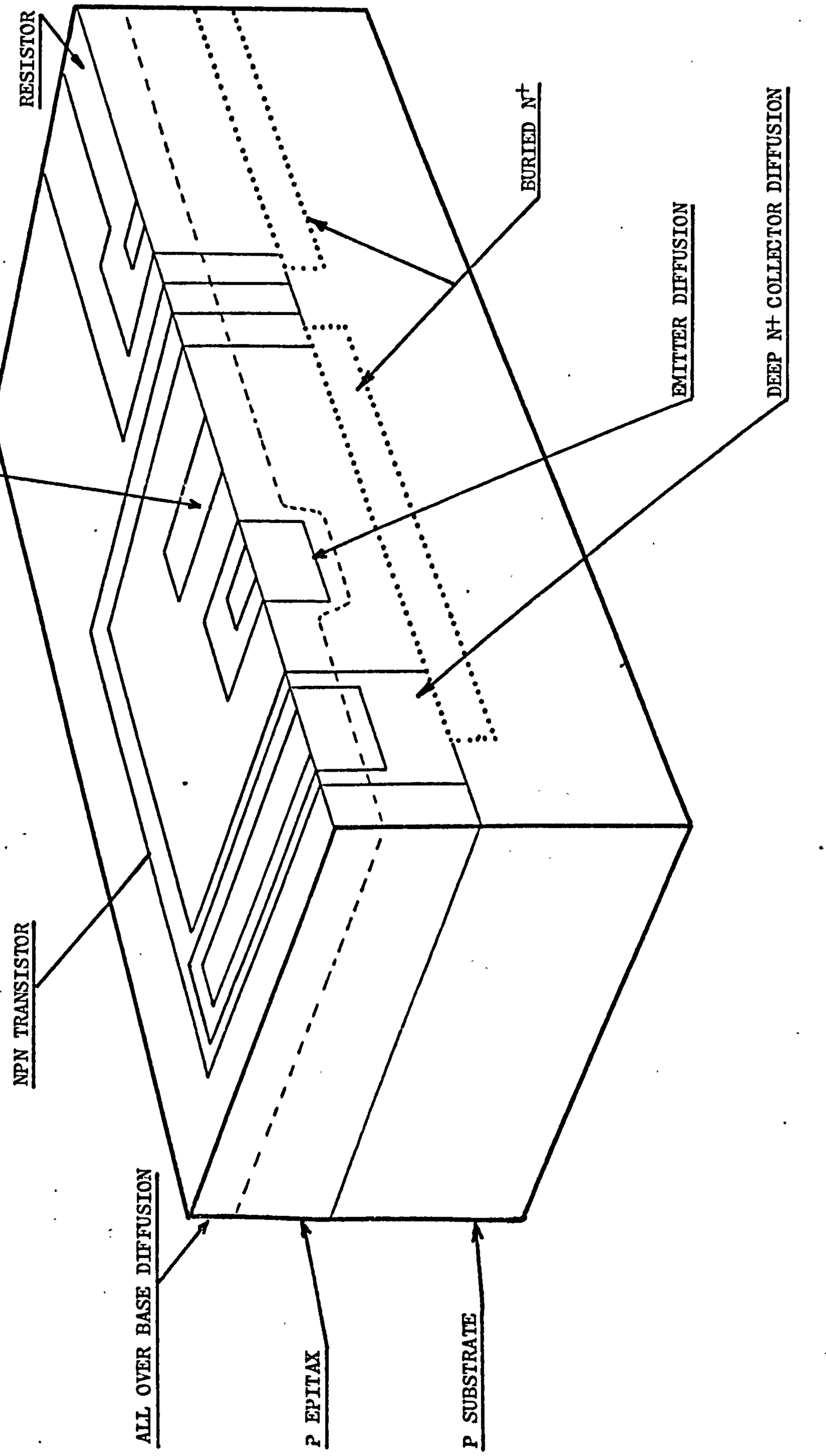


Figure 1.3.

BASIC COLLECTOR DIFFUSED ISOLATION STRUCTURE

epitaxial layer grown. A deep n^+ collector ring is diffused through the epitaxial layer to the buried N^+, thus forming an isolated p-type region of epitaxy. All oxides are removed and the surface receives a non selective boron diffusion. Emitters are then diffused. This results in a five mask epitaxial process. The CDI npn transistor has characteristics similar to a conventional planar epitaxial transistor. As the base diffusion intersects the deep collector diffusion, collector base breakdown voltages are degraded. The diffused/ epitaxial base structure results in a relatively poor frequency response.

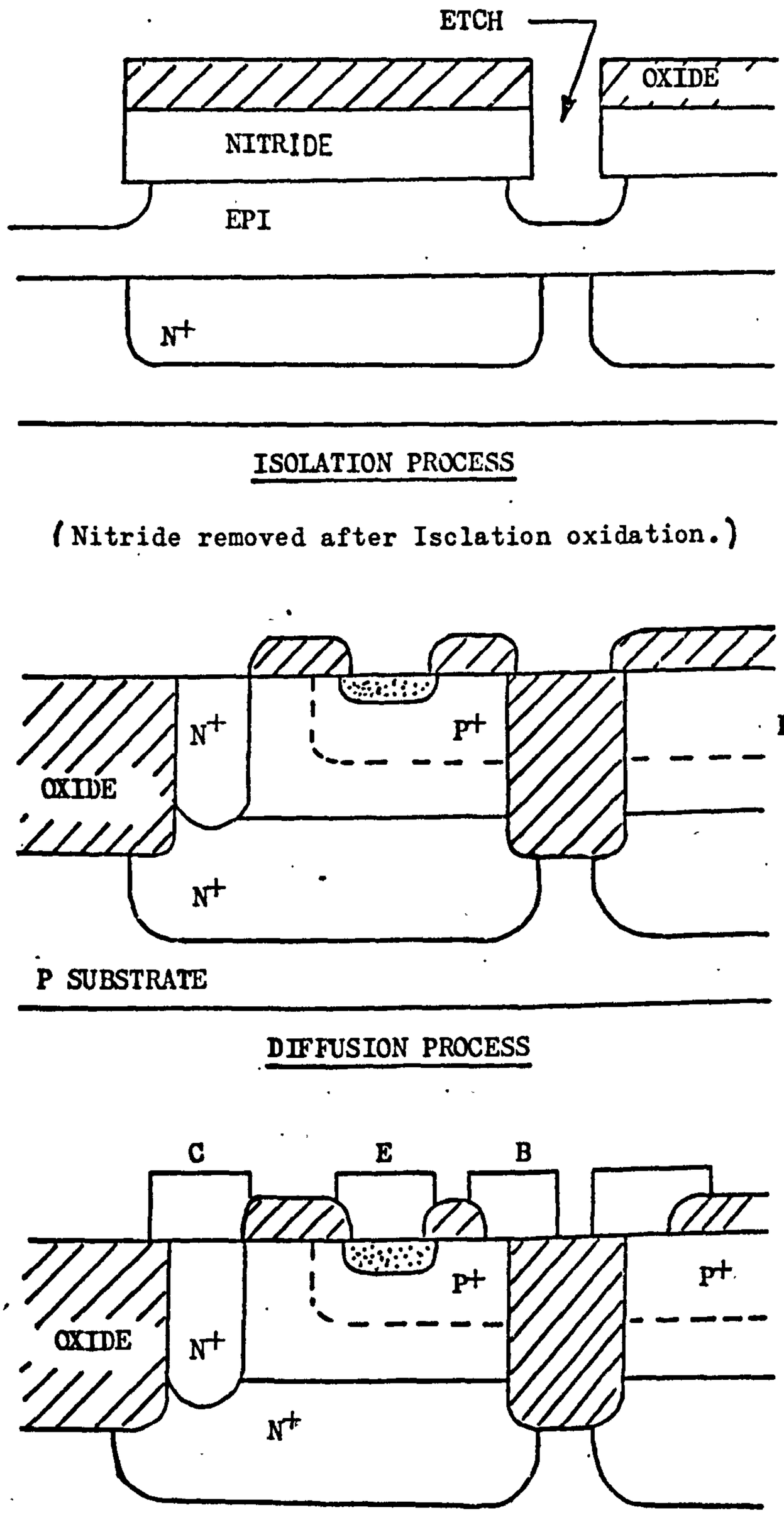
No pnp transistors are available on this process. However a p-channel junction FET can be fabricated using the intrinsic base region as a channel, and the emitter and buried N^+ regions as top and bottom gates.

1.1.3. Isoplanar

A concept similar to CDI is Fairchild's Isoplanar technology. This results in very high packing density and high performance. The processing technology is difficult, requiring silicon nitride deposition, selective etching and local oxidation, in addition to conventional planar technology requirememts. Figure 1.4. shows a simplified Isoplanar processing sequence. The local oxidation results in the minimum possible area occupied by isolation. No breakdown voltages are compromised as in CDI. Considerable problems are encountered where the oxide isolation intersects diffused regions. Inversion of the p-type epitaxial layer at the oxide interface is a problem:

Figure 1.4.

ISOPLANAR II PROCESSING



ISOLATION PROCESS

(Nitride removed after Isclation oxidation.)

DIFFUSION PROCESS

COMPLETED ISOPLANAR II DEVICE

Gallium can be diffused through the oxide to prevent this, and ion implantation can also be used.

Apart from complexity this technique is very attractive. Fairchild have published data (11) showing that novel pnp structures can be added to the Isoplanar process with modifications to the basic approach.

The most significant advantage of Isoplanar is an exceptionally high packing density and Fairchild have obviously sacrificed ease of production to achieve this goal.

1.2. INTEGRATED INJECTION LOGIC (I^2L)

In conventional planar epitaxial processes, apart from producibility, two major obstacles must be overcome before an LSI circuit can be fabricated. These are:-

(1) Planar epitaxial structures are not self isolating; large areas are consumed in producing isolation of active devices, and resistors.

(2) The area occupied by current defining resistors is prohibitive for low power circuits.

Figures 1.1. and 1.5. illustrate these points. Figure 1.5. also shows the basic I^2L structure. This can be considered as a derivative of DCTL and RTL (9,10). In I^2L the npn transistors are operated in the inverse mode, hence the Buried N^+ and epitaxial layer act as emitter, and the emitter diffusions as collectors. In inverted transistors collectors are self-isolating but emitters are common, base current is supplied directly as holes emitted from an adjacent p diffusion, which, together with the npn base as a collector forms a lateral pnp.

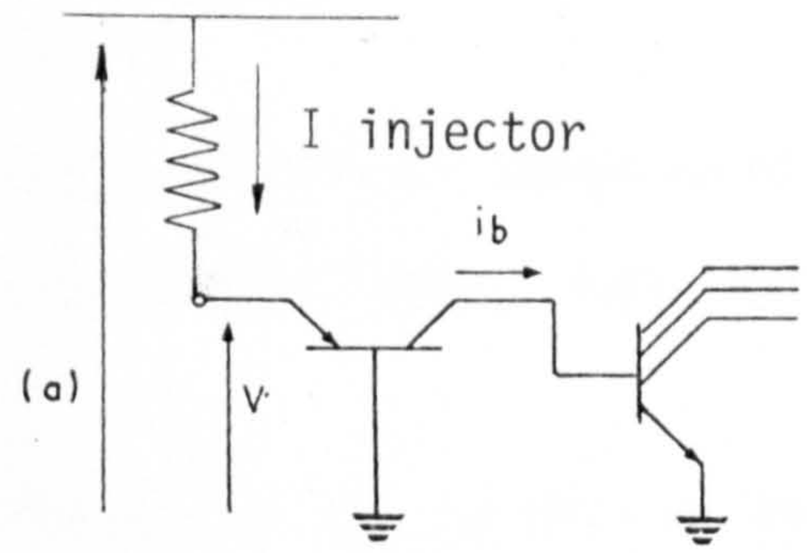


FIGURE 1.6

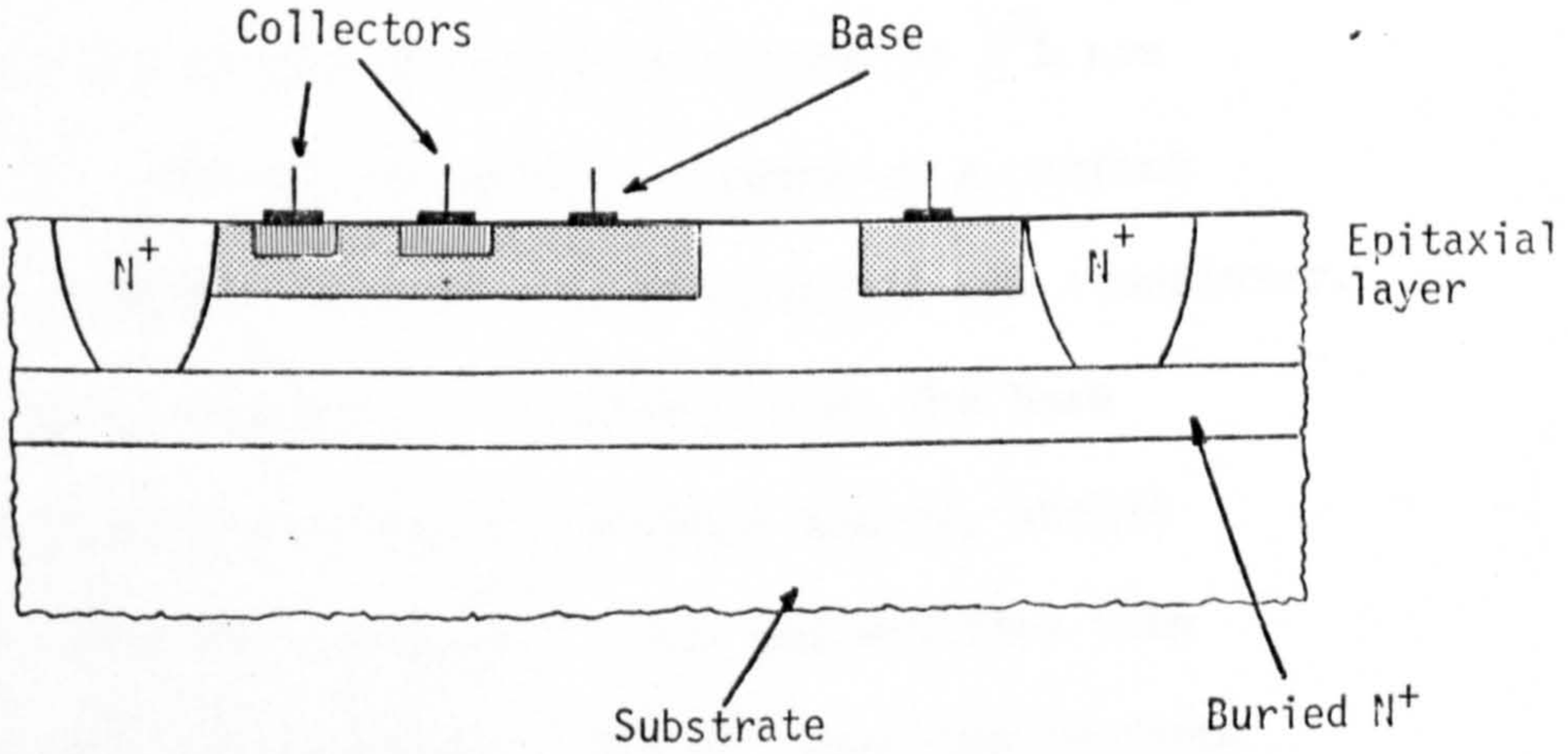


FIGURE 1.5

BASIC I^2L GATE

The emitter of the pnp is known as the injector. To avoid confusion the following nomenclature suggested by Weidmann and Berger (12) will be used:-

Parameters relating to inverse operation of the npn transistor will be described as upward mode, and identified with a subscript u.

Normal mode operation of the npn will be described as downwards mode and parameters identified with a subscript d. The subscripts n and i will be used to identify the pnp transistor operating in forward and inverse directions respectively.

The normal diffusion will be described as shallow N^+ diffusion and collector sinker diffusion* as Deep N+.

The simple equivalent circuit representations of I^2L are shown in Figure 1.6. The pnp transistor appears as a current source directly driving the base of a multicollector npn transistor. The I^2L gate is a super-integrated structure, i.e, the base of the npn is the collector of the pnp current source, whilst the npn emitter is also the pnp base. The pnp emitters (the injectors), are common to all gates. The I^2L gate has overcome the major disadvantages of planar bipolar technology, i.e. the device is self isolating, and the operating current is defined by a relatively small pnp transistor. Furthermore, this current is easily adjusted by changing the injector forward bias (V_{be}).

The operation of the I^2L gate is as follows: Consider the two identical gates T_1 and T_2 in Figure 1.7, in which the collector of the T_1 is connected to the base of the T_2 npn.

* Deep diffused N-type region from the silicon surface to the buried N+ region.

Basic Operation of I^2L.

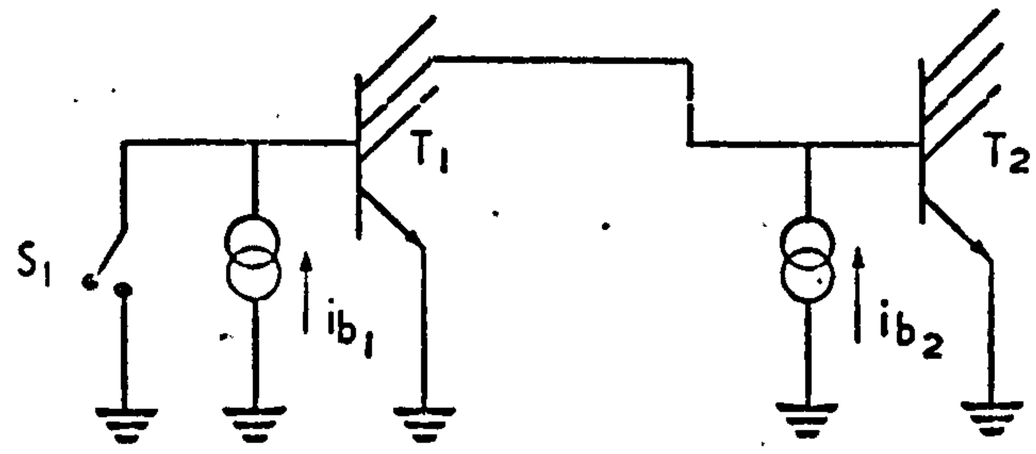
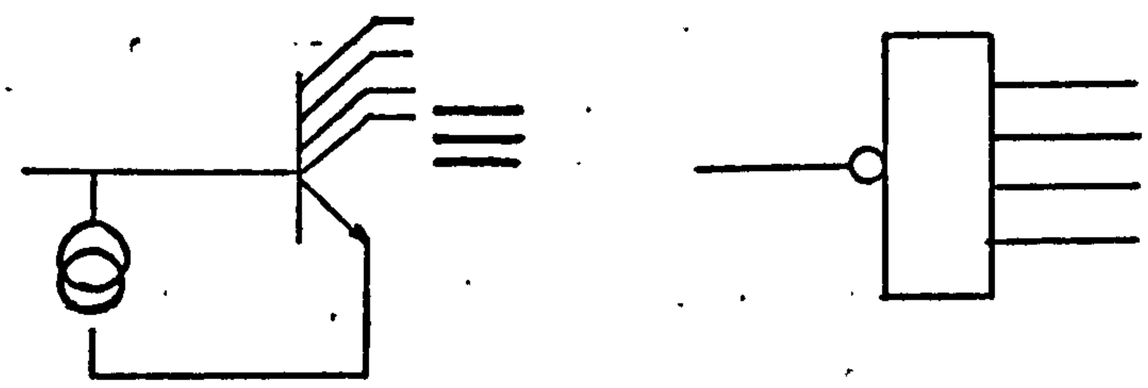
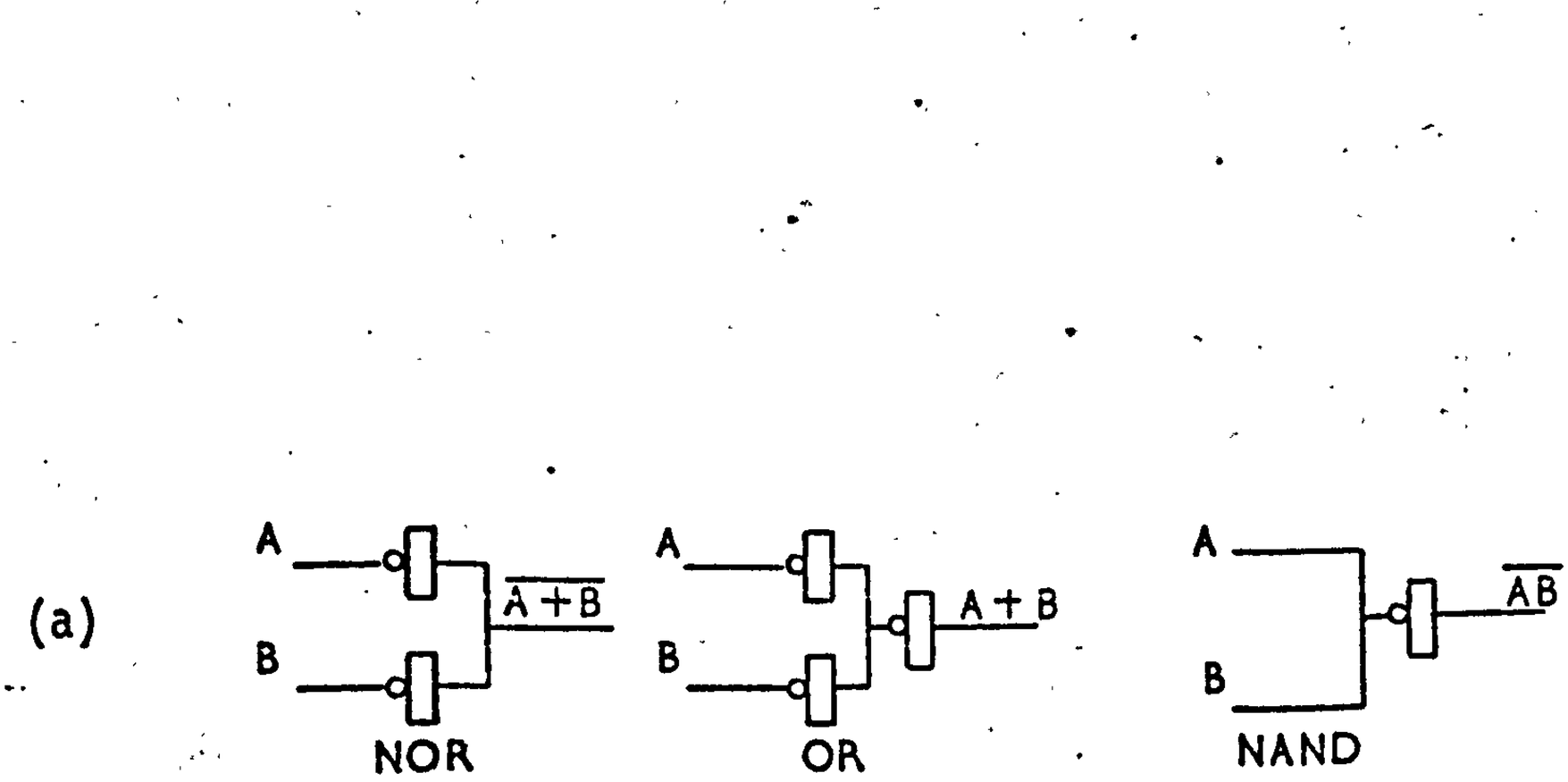


FIGURE 1.7





I^2L Logic Functions.

FIGURE 1.8

Both npn's have their associated pnp injectors and currents I_1 and I_2 are collected at each base respectively. If each npn has a gain of β_u, and $I_1 = I_2 = I_o$ (both pnp's identical), each collector is capable of sinking $\beta_u I_o$ collector current. Consider switch S_1 open; I_o will flow into base T_1, which will turn on and saturate if $\beta_u > 1$. The collector of T_1 will therefore sink all the base current of T_2, thus T_2 will be off. If S_1 is closed the base current of T_1 flows to ground, T_1 is off and T_2 is now on.

The basic requirement of the I^2L gate is an npn transistor with a common emitter current gain greater than unity. This is an over simplification as will be shown later, but it does illustrate the fact that I^2L is not very demanding on gain parameters. Reference to Figure 1.7 will show that no junction is operated at a potential of greater than a V_{be}, thus voltage requirements are trivial.

Figure 1.8a shows how logic functions may be implemented in I^2L. The interconnection of collectors results in a Wired-AND or NOR function. Figure 1.8b shows how this technique is used to implement a D-type flip-flop. (Each collector inverts the base signal).

I^2L is able to implement any logic function in spite of the single input multi output configuration. Figure 1.9 shows the logic diagram of 14-bit programmable pseudo random sequence generator designed by V. Blatt of The Plessey Company Limited. Figure 1.10 is a photograph of the implemented circuit using Plessey Bipolar Process III I^2L.

Logic Diagram I^2L Integrated circuit WM7.

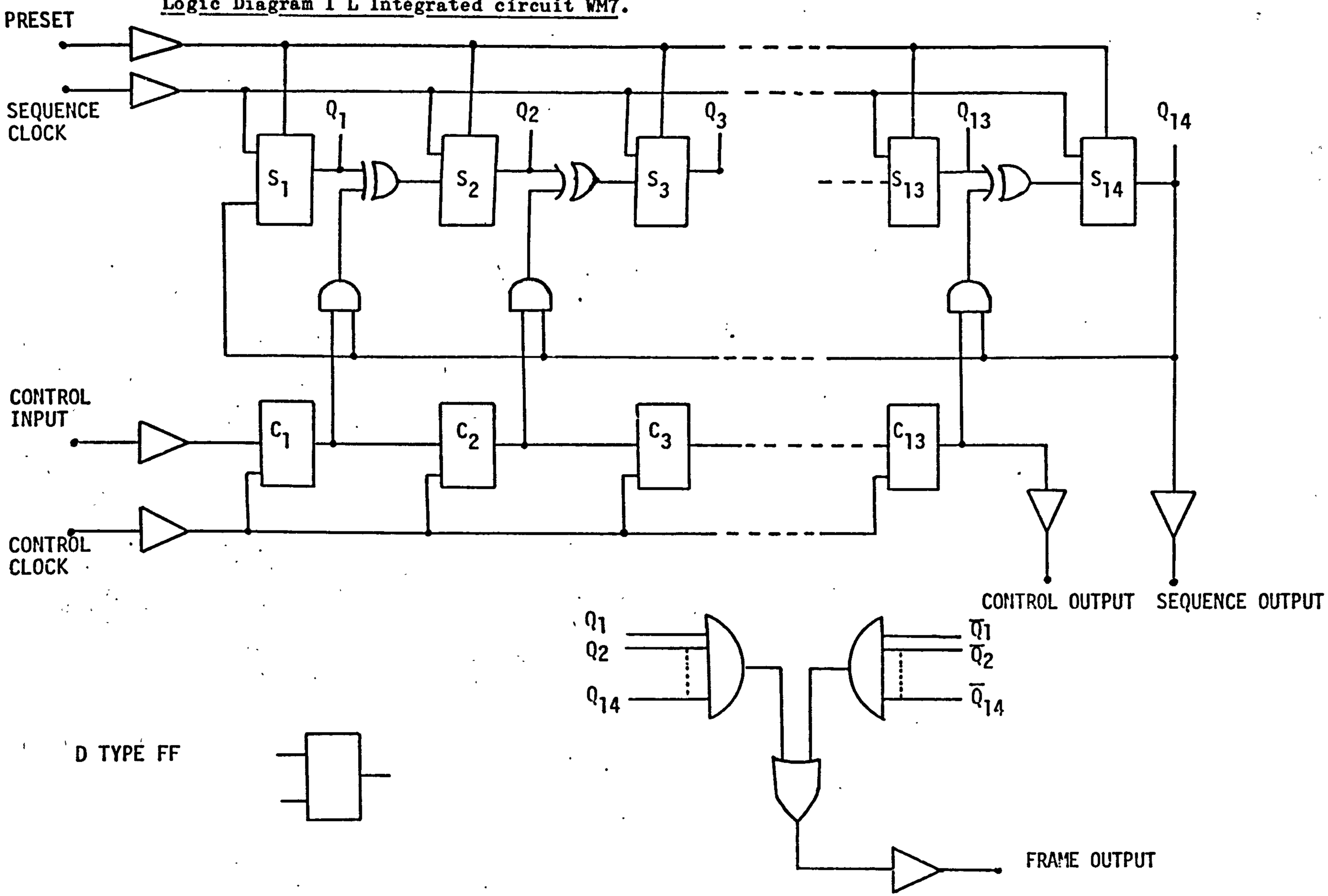


FIGURE 1.9

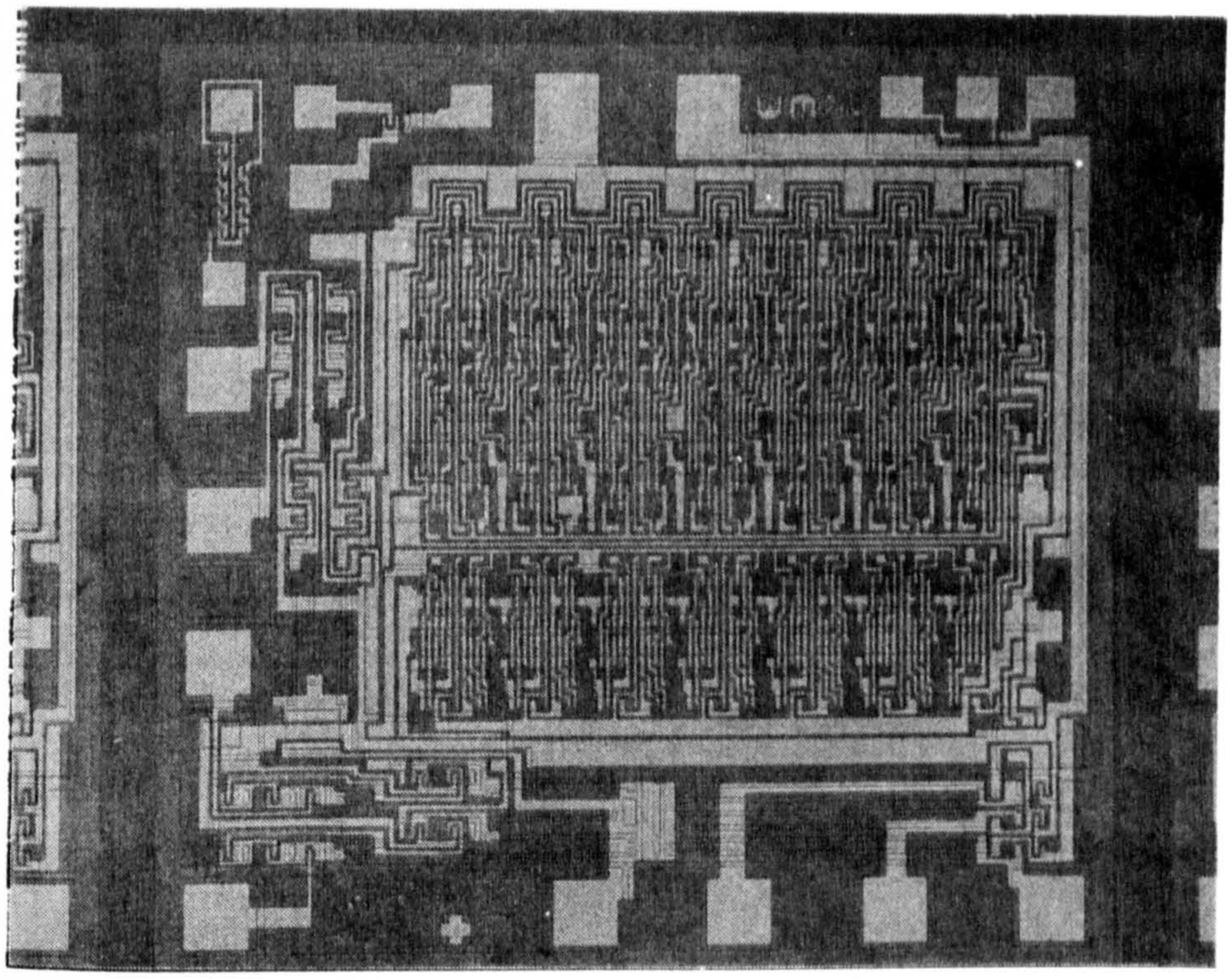


FIGURE 1.10 I^2L INTEGRATED CIRCUIT WM17

CHIP SIZE 73 x 70 THOU.

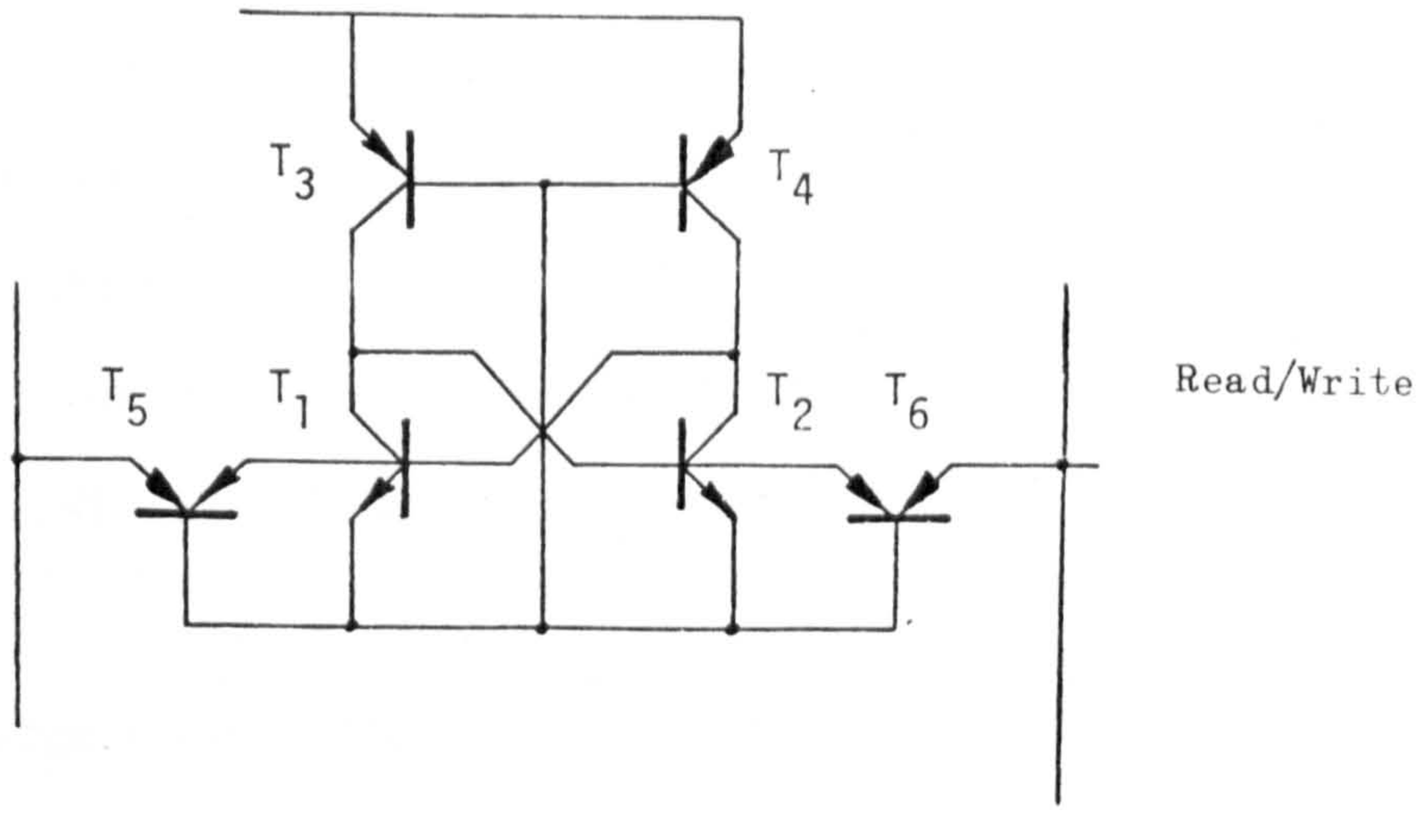


FIGURE 1.11

CIRCUIT DIAGRAM I^2L MEMORY CELL

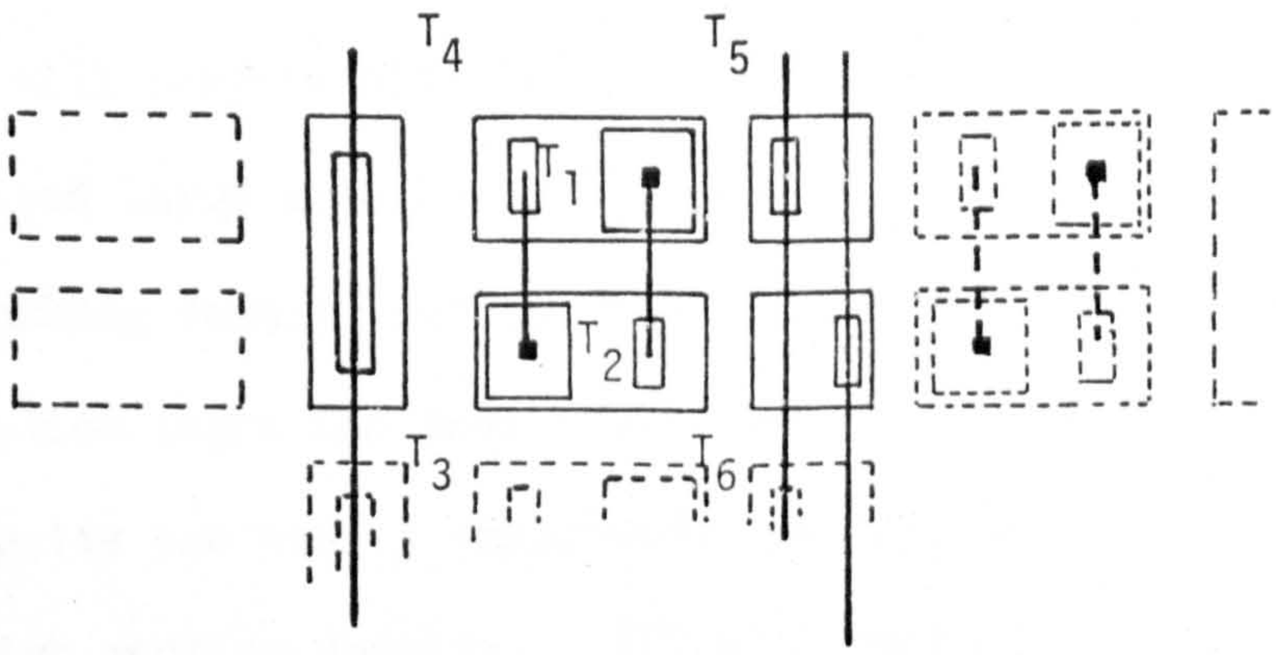


FIGURE 1.12

LAYOUT I^2L MEMORY AND ARRAY CONFIGURATION

I^2L can be used to implement memories, the memory cell of Weidmann and Berger (13) being one of the initial ideas leading to I^2L.

An I^2L memory cell is shown in Figure 1.11. (13). This cell uses super-integrated lateral pnps as loads for the latch. Information is written into and read from the cell using two more super-integrated lateral pnp's. Cell layout is shown in Figure 1.12. Access times of 50 ns ... and DC standby powers of 100 nW are quoted for a 4k bit RAM using this cell.

1.3. SUMMARY

The subject of large scale integrated bipolar circuits has been introduced. Pertinent requirements for such circuits have been discussed together with a limited comparison between various solutions to these problems. Generally the semiconductor industry has decided that simplified processing is the only way bipolar technologies will compete with MOS technologies. Low power operation required large area consuming resistors with consequent loss of packing density and increased yield hazard.

Integrated injection logic has been introduced. It has been shown that logic circuits are easily implemented using I^2L, and that I^2L has a high packing density. I^2L will operate with low inverse gain devices and is undemanding on voltages. It will be shown later that the technique has a low power delay product and is capable of operation to TTL speeds.

The major asset of I^2L is that the technique can be used on any planar epitaxial process, and thus improve the capability of that process. On a given process, analogue and digital

circuits can be implemented with I^2L on the same chip.

CHAPTER 2

BASIC OPERATION OF I^2L GATE

D.C. MODELS OF INTEGRATED INJECTION LOGIC GATES

2.1. INTRODUCTION

As described in Chapter 1 the I^2L gate is a superintegrated structure consisting of an upside down operated multicollector npn transistor whose base current is derived from a lateral pnp. Although the operation of this gate is basically simple its performance depends upon the interaction between the collectors of the saturating npn transistor and the effect of the pnp current source on the npn device must be adequately described. The current hogging effects between collectors must be quantified; the pnp transistor is saturated thus the pnp inverse gain can have a dominant effect on the characteristics of the npn transistor.

2.2. TERMINAL ORIENTED MODELS (i.e. from observation of terminal characteristics)

The terminal orientated I^2L gate model was proposed by Weidmann and Berger (12). Weidmann and Berger use the approach to calculate power consumption and to make elementary delay computations. The technique is at its most powerful in analysing DC operation and effects such as current hogging.

Figure 2.1. shows a 4 collector I^2L structure. Figure 2.1(a) is a schematic representation of the device whose equivalent circuit is shown in Figure 2.1(b). Using an extended Ebers-Moll approach the following representation can be derived.

The resultant junction current I_i crossing junction i is the

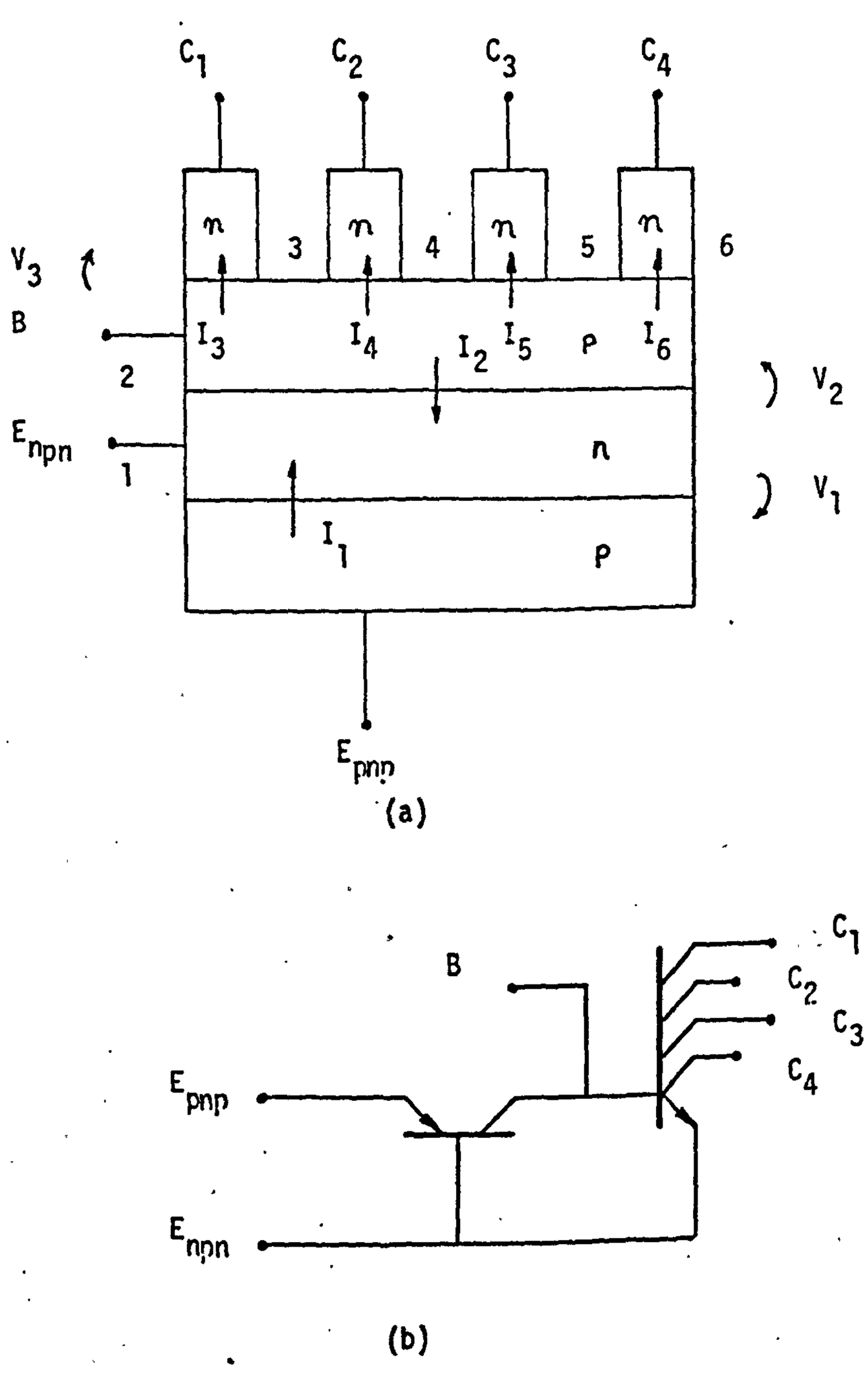


FIGURE 2.1

(All currents are those crossing a junction and are the sum of collected and injected currents)

linear superposition of partial currents I_{ik} being either injected (i = k) or collected ($i \neq k$) across the junction.

The injected current of the i^{th} junction (I_{ii}) is

$$I_{ii} = I_{io} \left(\exp q \frac{Vi}{KT} - 1\right)$$

obtained by shorting all other junctions.

The collected minority carrier current of the i^{th} junction is a fraction α_{ik} of the injected current at junction k which shares a region with the collecting junction.

$$I_{ik} = \alpha_{ik} I_{ko} \left(\exp q \frac{Vk}{KT} - 1\right)$$

$$= \alpha_{ik} I_{kk}$$

For the device of Figure 2.1. this results in the following matrix:

$$\begin{vmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{vmatrix} = \begin{vmatrix} 1 & \alpha_{12} & 0 & 0 & 0 & 0 \\ \alpha_{21} & 1 & \alpha_{23} & \alpha_{24} & \alpha_{25} & \alpha_{26} \\ 0 & \alpha_{32} & 1 & \alpha_{34} & \alpha_{35} & \alpha_{36} \\ 0 & \alpha_{42} & \alpha_{43} & 1 & \alpha_{45} & \alpha_{46} \\ 0 & \alpha_{52} & \alpha_{53} & \alpha_{54} & 1 & \alpha_{56} \\ 0 & \alpha_{62} & \alpha_{63} & \alpha_{64} & \alpha_{65} & 1 \end{vmatrix} \begin{vmatrix} I_{11} \\ I_{22} \\ I_{33} \\ I_{44} \\ I_{55} \\ I_{66} \end{vmatrix}$$

Zeros indicate positions where collection is impossible as junctions do not share a region.

If collectors C_1 C_2 C_3 C_4 are shorted to the base, $V_3 = V_4 = V_5 = 0$, the matrix reduces to ($I_{33} = I_{44} = I_{55} = 0$)

$$\begin{vmatrix} I_1 \\ I_2 \end{vmatrix} = \begin{vmatrix} 1 & \alpha_{12} \\ \alpha_{21} & 1 \end{vmatrix} \begin{vmatrix} I_{11} \\ I_{22} \end{vmatrix}$$

By alternately setting I_{11} and I_{22} to zero,

$$\alpha_{21} = \frac{I_2}{I_1} = -\alpha_n (V_2 = 0, \quad I_{22} = 0)$$

$$\alpha_{12} = \frac{I_1}{I_2} = -\alpha_i (V_1 = 0, \quad I_{11} = 0)$$

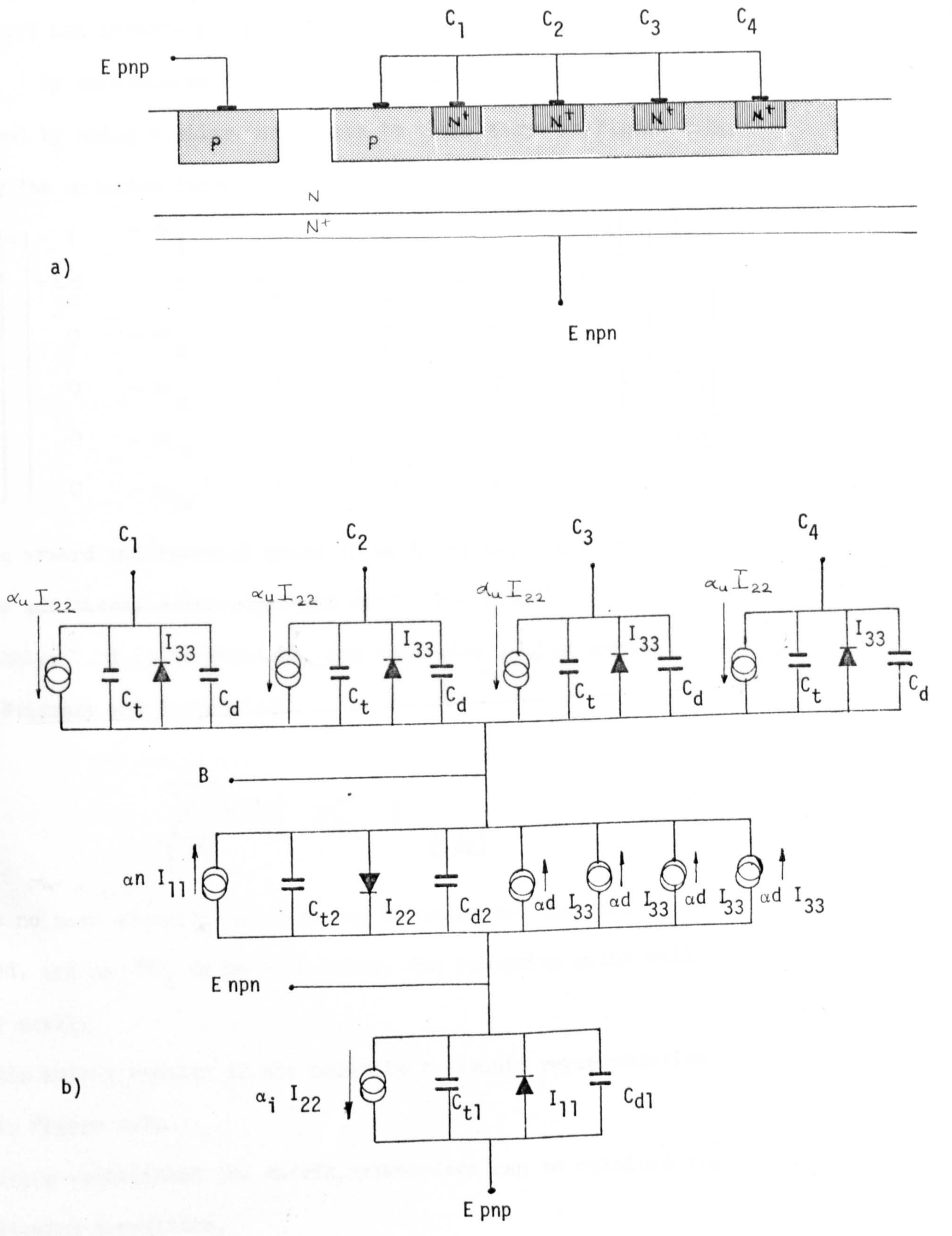


FIGURE 2.2. After Berger and Wiedmann

The forward and inverse pnp grounded base gains are thus defined. . By maintaining $V_1 = 0$ the remaining α 's may be determined by using similar techniques to those shown in Figure 2.2a. Adopting the notation introduced earlier:-

$$\begin{vmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{vmatrix} = \begin{vmatrix} 1 & -\alpha_i & 0 & 0 & 0 & 0 \\ -\alpha_n & 1 & -\alpha_d & -\alpha_d & -\alpha_d & -\alpha_d \\ 0 & -\alpha_u & 1 & 0 & 0 & 0 \\ 0 & -\alpha_u & 0 & 1 & 0 & 0 \\ 0 & -\alpha_u & 0 & 0 & 1 & 0 \\ 0 & -\alpha_u & 0 & 0 & 0 & 1 \end{vmatrix} \cdot \begin{vmatrix} I_{11} \\ I_{22} \\ I_{33} \\ I_{44} \\ I_{55} \\ I_{66} \end{vmatrix}$$

assuming upward and downward gains of each collector are identical.

The additional zeros represent conditions where collection is unlikely, that is between adjacent collectors. As pointed out by Weidmann and Berger (13).

$$\sum_{k=1}^{5} |\alpha_{ik}| \leqslant 1 \qquad (i \neq k)$$

because no more minority carriers may be collected than are injected, and as α_d is near to unity, the remaining gains will be very small.

This matrix results in the equivalent circuit representation shown in Figure 2.2b.

Having established the matrix, expressions can be obtained for the following quantities.

(1) Power consumption of a gate when the input is driven by the pnp transistor and the collectors are not sinking any

current, i.e. the npn transistor is in hard saturation.

(2) Power consumption by a gate in the off state.

(3) Power consumption by a gate when the input is driven and the collectors are sinking a current equal to the npn base current.

(4) The β u needed by a collector at the edge of saturation, in an n collector gate in order that the collector may sink twice its base current under the following conditions.

(a) All other collectors being open circuit and not sinking any current, i.e. hard saturation.

(b) All other collectors sinking a current equal to the base current of the npn.

These conditions correspond to the extremes of operation of an I^2L gate giving a reasonable noise margin. (An effective gain $\geq$ 2 will ensure that if a noise current pulse of equal magnitude to the base current is present at a collector incorrect information will not be propagated).

The above items will now be dealt with in turn.

Case 1.

Recognising that with no external input current

$$I_3 + I_4 + I_5 + I_6 = - I_2 = 0$$

and by definition $I_3 = I_4 = I_5 = I_6 = 0$

$$I_1 = I_{11} - \alpha_i \; I_{22} \qquad 2.1.$$

$$I_2 = - \alpha_n \; I_{11} + I_{22} - 4 \alpha_d \; I_{33} \qquad 2.2$$

$$I_3 = - \alpha_u \; I_{22} + I_{33} \qquad 2.3$$

$$I_4 = - \alpha_u \; I_{22} + I_{33} \qquad 2.4.$$

($I_n = - \alpha_u \; I_{22} + I_{33}$ for an n collector gate since areas of collectors are equa

Using $I_{33} = \alpha_n \; I_{22}$ we obtain in equation 2.2, $I_3 = 0$ by definition.

$$I_2 = -\alpha_n I_{11} + I_{22}(1-4\alpha_d \alpha_u) \qquad 2.5$$

$$\therefore \quad I_{22} = \left(\frac{I_{11}\alpha_n}{(1-4\alpha_d \alpha_u)}\right)$$

substituting 2.5 into 2.1.

$$I_1 = I_{11}\left(\frac{(1-\alpha_n \alpha_i)}{(1-4\alpha_d \alpha_u)}\right) \qquad 2.6.$$

Now I_1 = injector current.

If V_1 is injector voltage, then

$$\text{Power} = V_1 I_{11}\left(\frac{(1-\alpha_n \alpha_i)}{(1-4\alpha_d \alpha_u)}\right) \qquad 2.7a.$$

For an n collector device,

$$\text{Power} = V_1 I_{11}\left(\frac{(1-\alpha_n \alpha_i)}{(1-n\alpha_d \alpha_u)}\right) \qquad 2.7b.$$

Case 2

The base current is diverted to ground by the collector of another gate; only the injector junction is forward biased and all other junctions are effectively zero biased. Thus the power consumed is

$$\text{Power} = V I_{11}$$

Case 3

Each npn collector of the "on" gate is normally required to sink the pnp collector current, i.e. $\alpha_n I_{11}$. Assuming the injector bias is constant for each gate and pnp's are identical, then

$$I_1 = I_{11} - \alpha_1 I_{22} \qquad 2.8.$$

$$I_2 = -\alpha_n I_{11} + I_{22} - 4\alpha_d I_{33} \qquad 2.9$$

$$I_3 = -\alpha_u I_{22} + I_{33} \qquad 2.10.$$

$$I_4 = -\alpha_u I_{22} + I_{33} \qquad 2.11.$$

etc

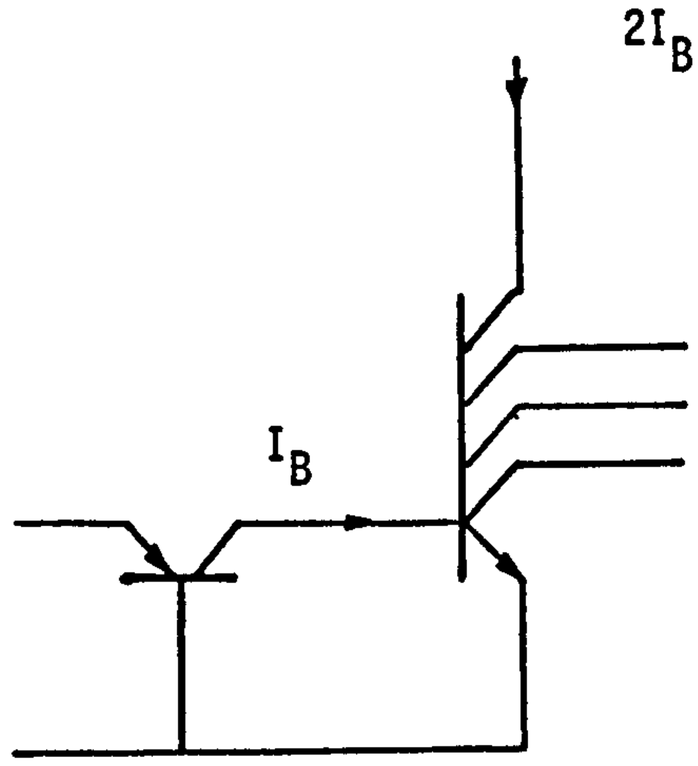


FIGURE 2.3

I^2L gate with twice base current in one collector.

Collector current is $-\alpha_n I_{11} = I_3 = I_4 = I_5 = I_6$ 2.12.

Since there is no external base current

$$I_3 + I_4 + I_5 + I_6 = I_2 \quad 2.13$$

$$I_2 = +4\alpha_n I_{11} \quad 2.14.$$

$$-\alpha_n I_{11} = -\alpha_u I_{22} + I_{33} \quad 2.15$$

$$I_{33} = \alpha_u I_{22} - \alpha_n I_{11} \quad 2.16$$

Substituting 2.16. and 2.14. into 2.9. gives

$$I_{22} = I_{11} \frac{(5\alpha_n - 4\alpha_n \alpha_d)}{(1-4\alpha_d \alpha_u)}$$

Using 2.8.

$$I_1 = I_{11}\left(1 - \frac{\alpha_i(5\alpha_n - 4\alpha_n \alpha_d)}{(1 - 4\alpha_d \alpha_n)}\right.$$

For an n collector gate this becomes

$$I_1 = I_{11}\left(1 - \frac{\alpha_i \alpha_n((n+1) - n\alpha_d)}{(1 - n\alpha_d \alpha_u)}\right.,$$

giving the power consumption as

$$P = V_1 I_{11}\left(1 - \frac{\alpha_n \alpha_i((n+1) - n\alpha_d))}{(1 - n\alpha_d \alpha_u)}\right.$$

Case 4a

Consider a four collector gate with base current I_B and one collector at the edge of saturation, (collector current $2I_B$.) and other collectors are logically interconnected with other gates, thus many npn collectors may be sharing one pnp collector current. Assuming the worst case of an infinite number of gates connected to the base, the other npn collectors will have no collector current (Figure 2.3). The pnp collector current is $-\alpha_n I_{11}$, npn collector current is $-2\alpha_n I_{11}$.

Now,

$$I_1 = I_{11} - \alpha_i I_{22}$$

$$I_2 = -\alpha_n I_{11} + I_{22} - \alpha_d I_{33} - \alpha_d I_{44} - \alpha_d I_{55} - \alpha_d I_{66}$$

$$I_3 = -\alpha_u I_{22} + I_{33} = 0$$

$$I_4 = I_5 = I_3 = 0$$

If collector 4 is conducting at the edge of saturation, it injects zero current, therefore

$$I_6 = -\alpha_u I_{22}$$

(Since $I_{66} = 0$)

$$I_6 = -2\alpha_n I_{11}$$ (twice pnp collector current)

As

$$I_3 = I_4 = I_5 = 0 \qquad \alpha_u I_{22} = I_{33}$$

$$-I_2 = I_6$$

,

$$I_2 = -\alpha_n I_{11} + I_{22} - 3\alpha_d I_{33}$$

$$3\alpha_n I_{11} = I_{22}(1 - 3\alpha_d \alpha_n)$$

Substituting now

$$\alpha_u I_{22} = 2\alpha_n I_{11}$$ from conducting collector

$$\alpha_u = \frac{2}{(3 + 6\alpha_d)}$$

For an n collector gate

$$\alpha_u = \frac{2}{(3 + 2(n-1)\alpha_d)}$$

From the definition of α_u as the fractional α associated with an individual collector, the β_u associated with the collector is

$$\frac{\alpha_u}{1-n\alpha_u}$$

Rearranging and substituting for β_d gives

$$\beta_u = \frac{2(\beta_d + 1)}{\beta_d + 3 - 2n} \qquad \left(\beta_d = \frac{\alpha_d}{1-\alpha_d}\right)$$

This is plotted as a function of n in Figure 2.4.

Case 4b

Using similar arguments to case 4a but with the exception of saying that on an n collector gate n-1 collectors are sinking an input current and the remaining collector is required to sink twice an input current.

$$\beta_u = \frac{\beta_d + 1}{\beta_d + 2 - n}$$

This expression is plotted in Figure 2.5. as a function of n.

The results shown in Figures 2.4.and 2.5. indicate that if β_d is not large a β_u considerably larger than two is required, if a collector is to sink in excess of twice its base current. Figure 2.5. shows the worst case condition when many collectors are pulling down one base. β_d decreases with decreasing I_C usually due to increasing depletion region recombination, and β_u usually decreases for the same reason. Thus as I_C is decreased a critical condition appears where both β_u and β_d are decreasing. Although β_u could be larger than 2, the gate may develop into a state where its noise margin is inadequate.

2.3. INJECTION MODEL

The terminal model previously described with the addition of depletion and diffusion capacitance parameters has been used in circuit analysis work. However, it is obvious that the terminal model offers little insight into the parameters

Figure 2.4.

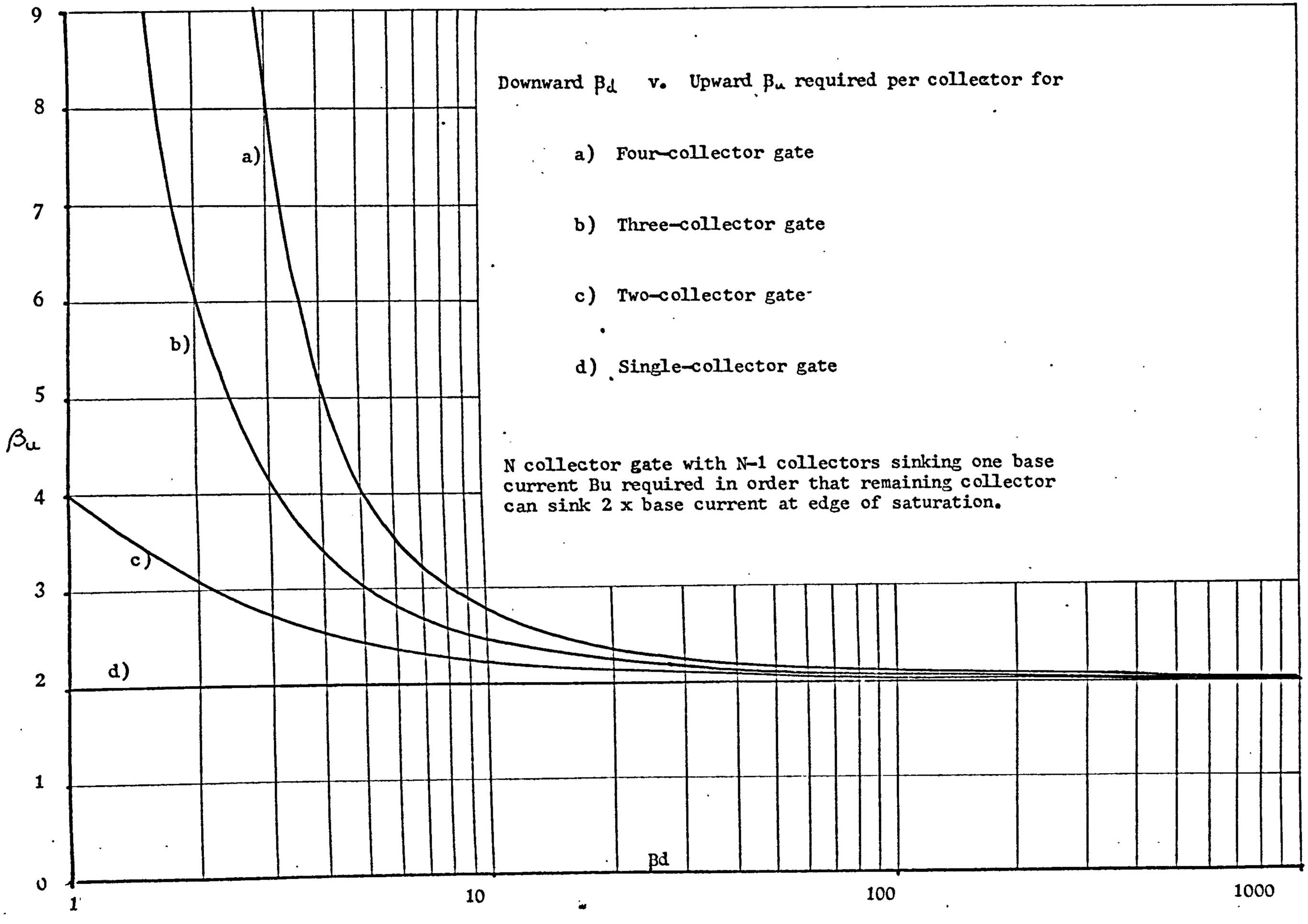
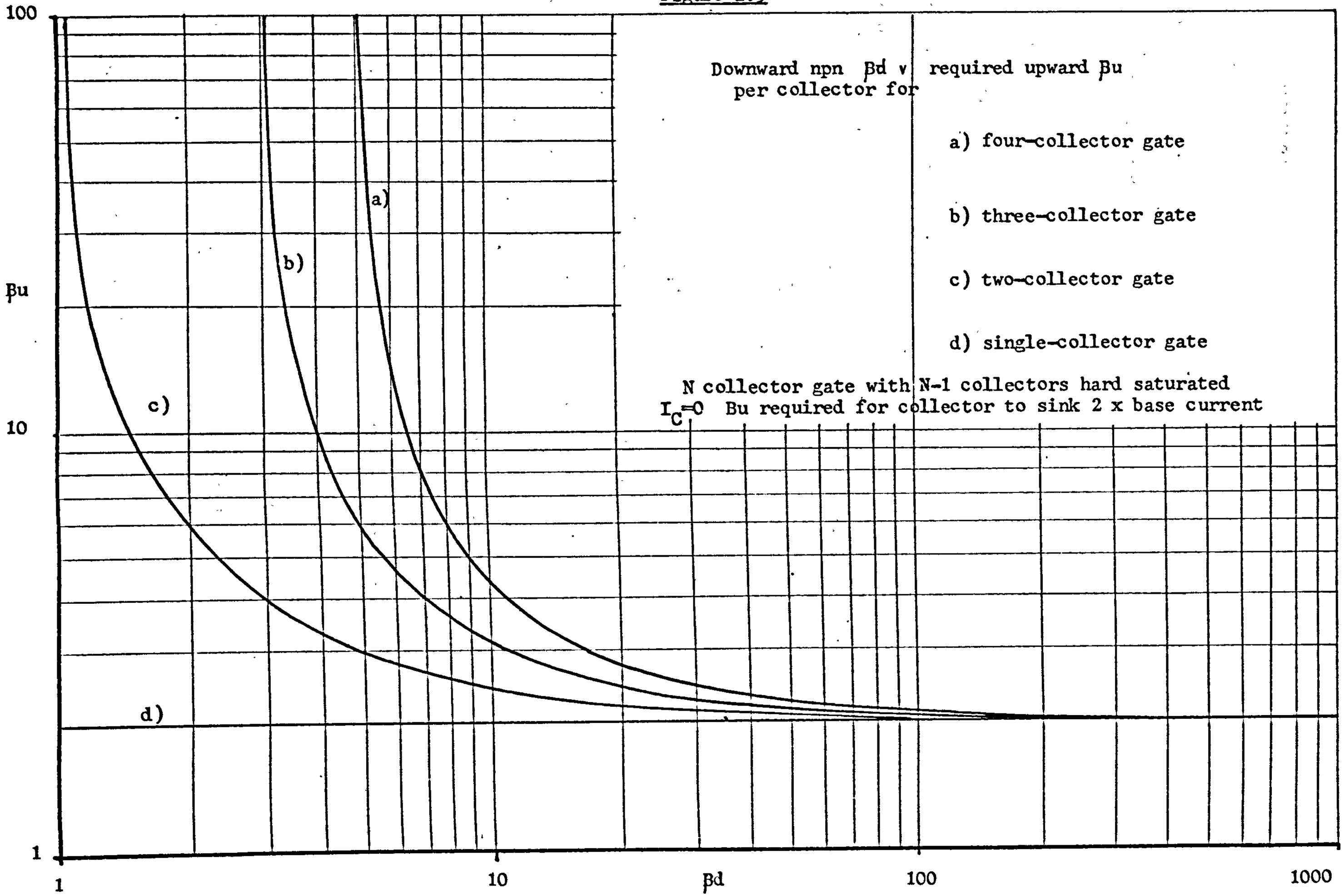

9
8
7
6
5
4
3
2
1
0
βu
a)
b)
c)
d)
1
10
100
1000
βd
Downward βd v. Upward βu required per collector for
a) Four-collector gate
b) Three-collector gate
c) Two-collector gate
d) Single-collector gate
N collector gate with N-1 collectors sinking one base current Bu required in order that remaining collector can sink 2 x base current at edge of saturation.

Figure 2.5


100
βu
10
1
1
10
βd
100
1000
a)
b)
c)
d)
Downward npn βd v required upward βu per collector for
a) four-collector gate
b) three-collector gate
c) two-collector gate
d) single-collector gate
N collector gate with N-1 collectors hard saturated
I_C=0 Bu required for collector to sink 2 x base current

controlling device behaviour. To rectify this, Berger (14) proposed the injection model. This model offers a considerably improved approach over the terminal model, and it is now possible to include debiasing effects associated with base resistance. F.M.Klaasen (15) has presented a model based on the device physics of I^2L and in essence the results are the same as those of Berger. Wulms (16) has suggested that some of the measurement techniques proposed by Berger are inadequate, and suggests an alternative measurement technique. However his results only add detail to the model proposed by Berger.

The injection model represents the injection logic device by considering the nature of the various hole and electron injections. The model as presented by Berger is based on experimental results. The magnitudes of the various injections are determined experimentally, and no attempt is made to relate these results to doping profiles or other physical parameters.

The structures used to obtain the magnitudes of the various currents are shown in Figure 2.6. These include a complete I^2L gate, and I^2L gate with shallow n^+ diffusions omitted, and a structure using all the base surface as contact.

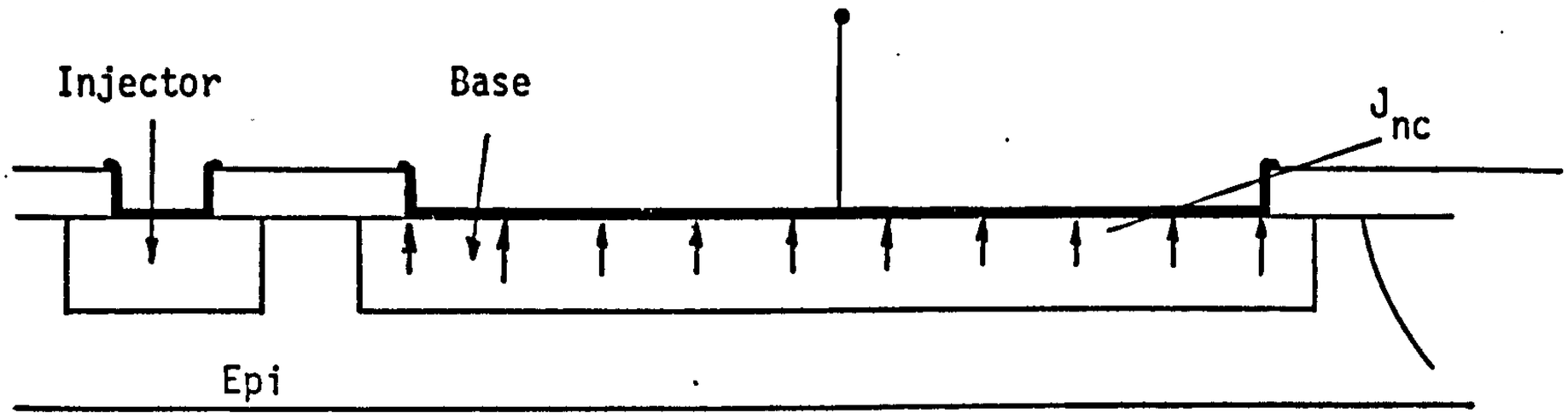
The following currents are obtained by applying a given V_{be} to the base-epitaxial junction of the structures shown in Fig 2.6.

Structure 1

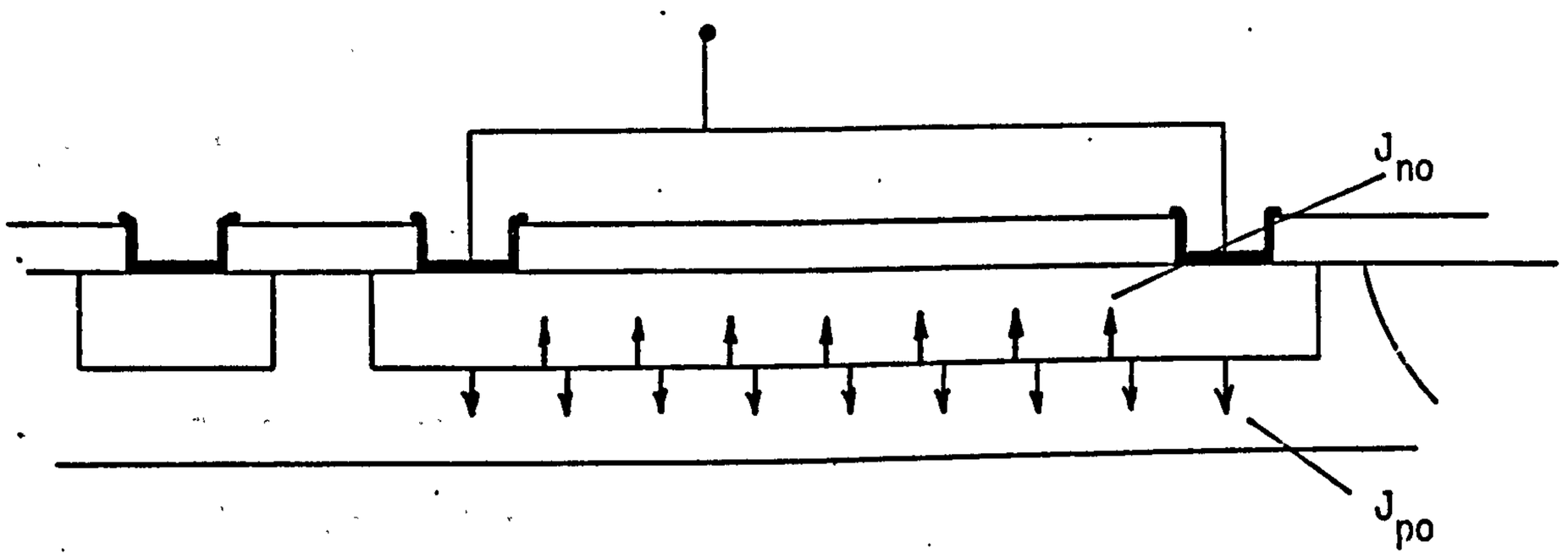
$$I_B = A_B . J_{PO} + (A_B - 3A_C - A_M) . J_{NO}$$

$$+ A_M . J_{NC} + L . J_{PL}$$

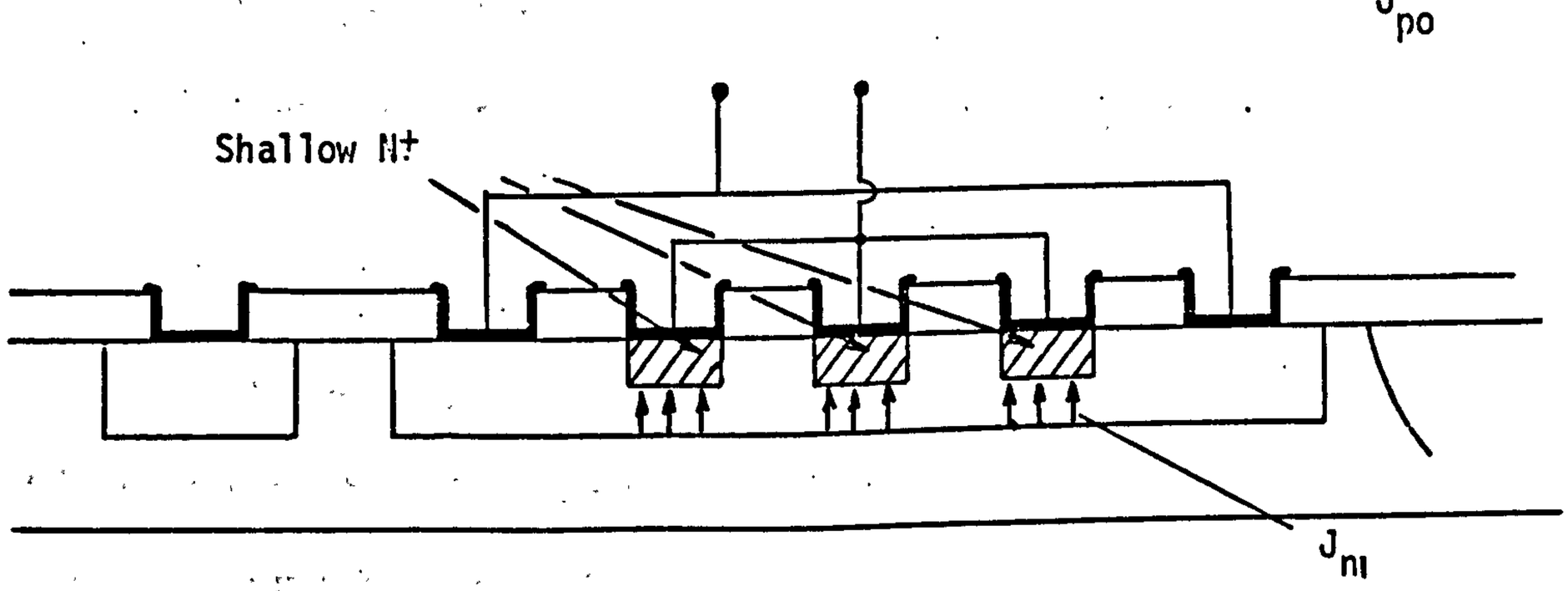
1.



2.



3.



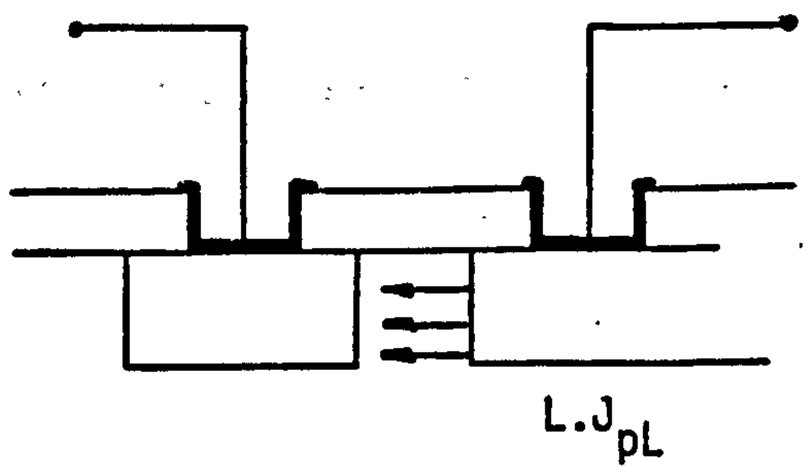


FIGURE 2.6

Injected currents in the I^2L gate.

Structure 2

$$I_B = A_B . J_{PO} + (A_B - A_M .) \; J_{NO}$$

$$+ A_M . \; J_{NC} + L . \; J_{PL}$$

Structure 3

$$I_B = A_B = J_{PO} + A_B . \; J_{NC} + L . \; J_{PL}$$

The collector current in structure 1 is

$$I_C = 3 . \; A_C . \; J_{ni}$$

Thus J_{PO} J_{NC} J_{NO} J_{ni} can be determined by solving these equations simultaneously, L x J_{PL} can be directly measured, and hence J_{PL} can be calculated.

Once the values of the current densities are known together with values of intercollector resistance it is possible to model an I^2L gate of any desired geometry. It is, of course, necessary to measure downward transistor characteristics for complete Ebers-Moll modelling. Figure 2.7. shows the various magnitudes of currents determined by this analysis.

Wulms (16) discovered that the phosphorus emitter diffusion affected the minority carrier recombination parameters, and that varying the surface area of the phosphorus diffusion in relation to that of base area altered the magnitude of the various currents previously described. This effect had been foreseen but was not observed on Process III structures.

The use of the Berger type structures to determine the various injection current densities is by necessity confined to regions where debiasing effects are not important. This means low current measurements, where depletion region recombination is important. Even at quite modest base currents depletion

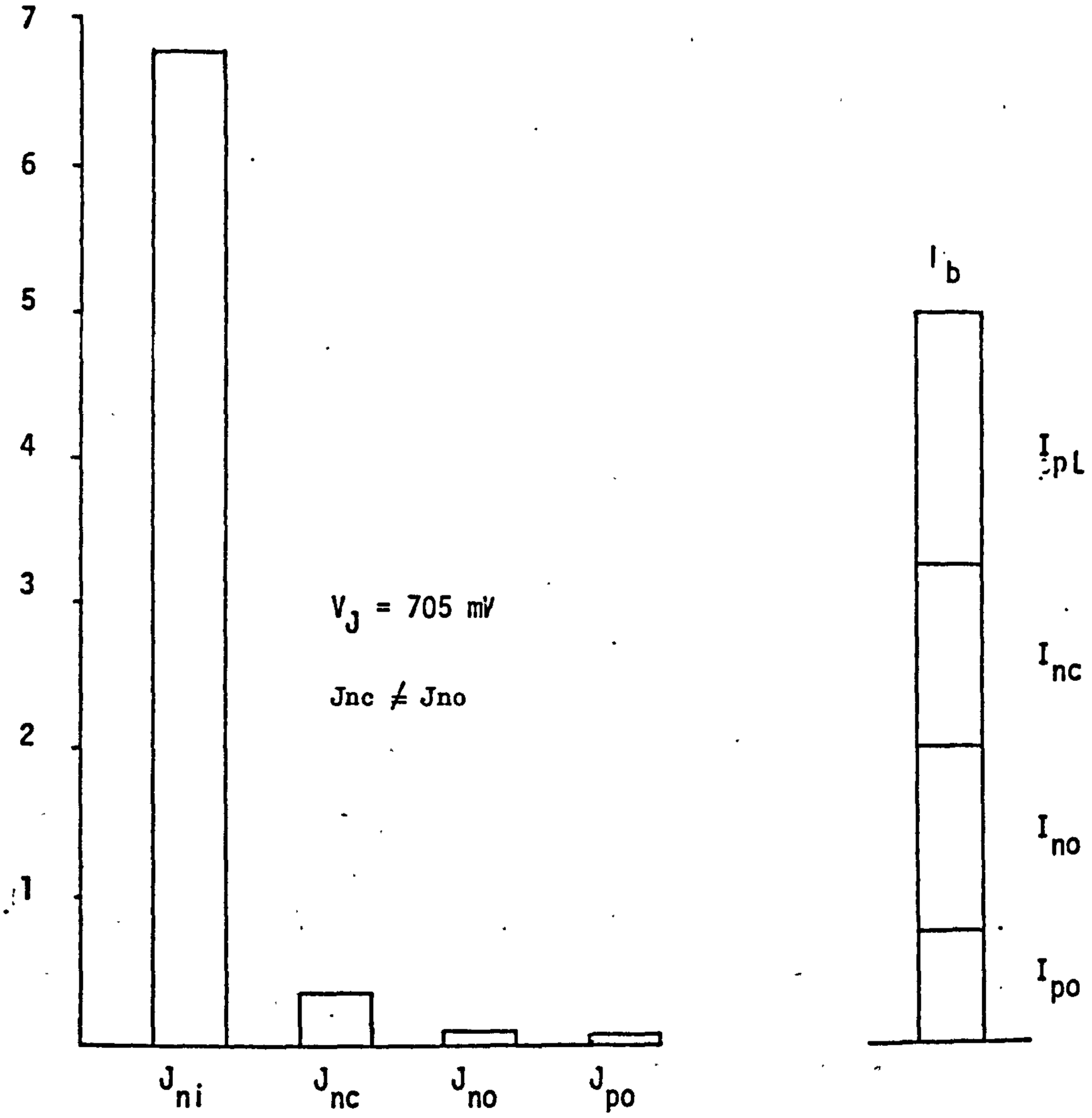


FIGURE 2.7

(a) Magnitude of injected current densities

(b) 10 μA total base current portioned according to injection mechanisms

After H.H. Berger

region recombination can be significant. This is the major criticism of this injection model, viz. depletion region recombination is not analysed.

SUMMARY

The terminal and injection models described are essentially observational tools. The terminal model allows the solution of simple Ebers-Moll type problems of the saturated super-integrated I^2L gate and shows easily the complex interactions of the many regions of the devices. The injection model leads to an understanding of the physical phenomena controlling device behaviour; for example injection into contact regions is shown to be different from that into oxide covered regions. Injection into the epitax is of the same order as that into base regions covered by oxide. However only limited basic insight into the mechanisms governing device behaviour is achieved, and it is not possible to predict how an I^2L gate will behave on a completely unknown process. This is the aim of the analysis developed in Chapters 3 and 4.

CHAPTER 3

COMPREHENSIVE INJECTION MODEL OF THE I^2L GATE

3.1. INTRODUCTION

The purpose of this chapter is to develop a model which describes the phenomena which control the behaviour of the I^2L gate. The analyses presented are not necessarily the most rigorous. However, they have proved more than adequate in describing the behaviour of I^2L gates fabricated on three processes. The injection model proposed by Berger listed the following base current components: (see Figure 2.6.)

J_{NC} - electron current injected into base regions covered by a metallic contact

J_{NO} - electron current injected into base regions covered by oxide

J_L - lateral injection associated with the saturated pnp injector transistor

J_{PO} - hole injection into the epitaxy/buried N^+ structure.

To Berger's set the depletion region recombination terms must be added;

J_{DL} - depletion recombination at the surface of the base junction

J_{DA} - depletion recombination associated with the base epitaxy junction.

An accurate description of the collector current is also necessary,

J_{ni} - collector current of (inverse) upward npn transistor.

The junctions will be assumed to be abrupt and dopings within a region to be uniform. Approximate analytic expressions will be

derived for each of these current terms.

Boltzmann statistics will be assumed in these derivations as will the concepts of steady state quasi-equilibrium. It is also assumed that applied forward biases are always larger than 3KT/q. The vertical current flow in the I^2L structure is related to that of a P^+NN^+ diode. These structures have been extensively analysed in the literature (17). However, most of the published work is not applicable in detail to the I^2L case, because

(a) The low doped region of the epitaxy is very narrow.

(b) The P^+NN^+ diode is a very high injection level device (18).

(c) Majority and minority currents are not necessarily comparable.

(d) The I^2L gate is a more complex structure.

The doping NN^+ interface region of the P^+NN^+ diode has been shown to be a blocking barrier. That is minority carrier accummulation takes place on the low doped side of the interface, resulting in reduced current flow and increased charge storage (19,20).

3.2. BASE CURRENT OF THE UPWARD NPN TRANSISTOR

3.2.1. Injected minority carrier level in epitaxy at the edge of the depletion region of the P^+ epitaxy junction

As the epitaxy is relatively lowly doped ($10^{16}cm^{-3}$) it moves into high level injection at low biases and the high level injection parameters of this region play a dominant part in device behaviour. The following analysis will assume that the

N^+ and P^+ regions do not enter high level injection. (This is beyond the regime in which the device will be operated).

At zero bias the N-type regions (N, epitaxy buried N^+) will have an electrostatic potential induced across them which is derived thus:-

Since $J_n = 0$ (by definition)

Then $$q\mu_n n E = -q D \frac{dn}{dx}$$

Let V_{SO} = zero bias electrostatic potential, then

$$V_{SO} = \int E \, dx = \frac{KT}{q} \int_{N_{EPI}}^{N^+} \frac{dn}{n}$$ (using the Einstein relationship)

$$V_{SO} = \frac{KT}{q} \ln \frac{N_{EPI}}{N^+}$$

In Figure 3.1. is shown a schematic of the potential and space charge associated P^+NN^+ structure.

If V_{APP} is the bias applied to the structure, then ignoring ohmic voltage drops under injection conditions, a part V_S of the bias will appear across the minority carrier gradient. If V_J is the junction voltage then $V_{APP} = V_S + V_J$.
If the hole and electron gradients are equal then a potential V exists between the buried N+ and the edge of the pn junction depletion region.

$$E = \frac{-KT}{q} \frac{1}{n} \frac{dn}{dx}$$

and $$V = \frac{KT}{q} \ln \frac{n}{N^+}$$

Subtracting zero bias electrostatic potential gives

$$V_S = + \frac{KT}{q} \ln \frac{n}{N_{EPI}}$$

where n is the electron level at the edge of the depletion layer

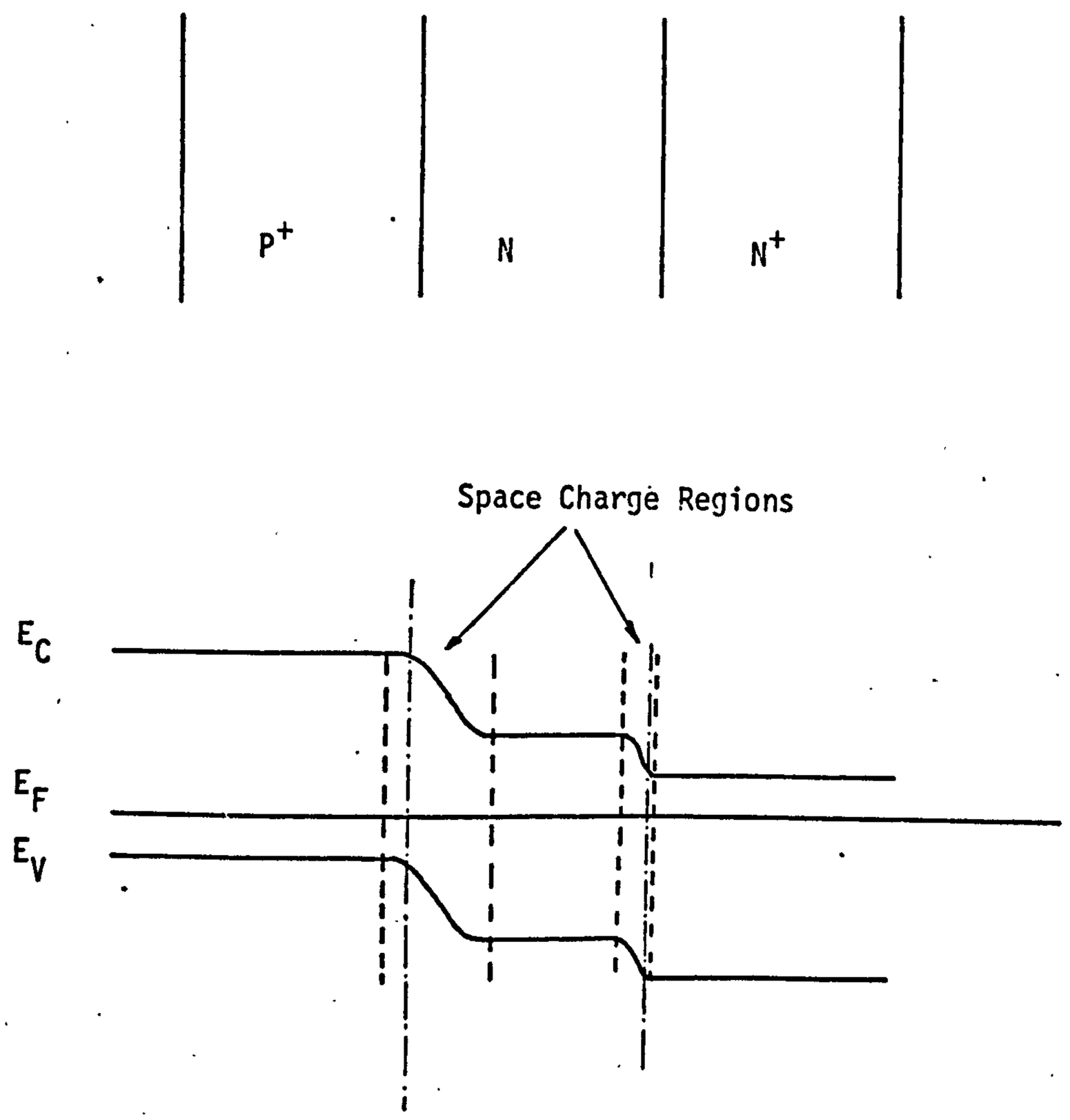
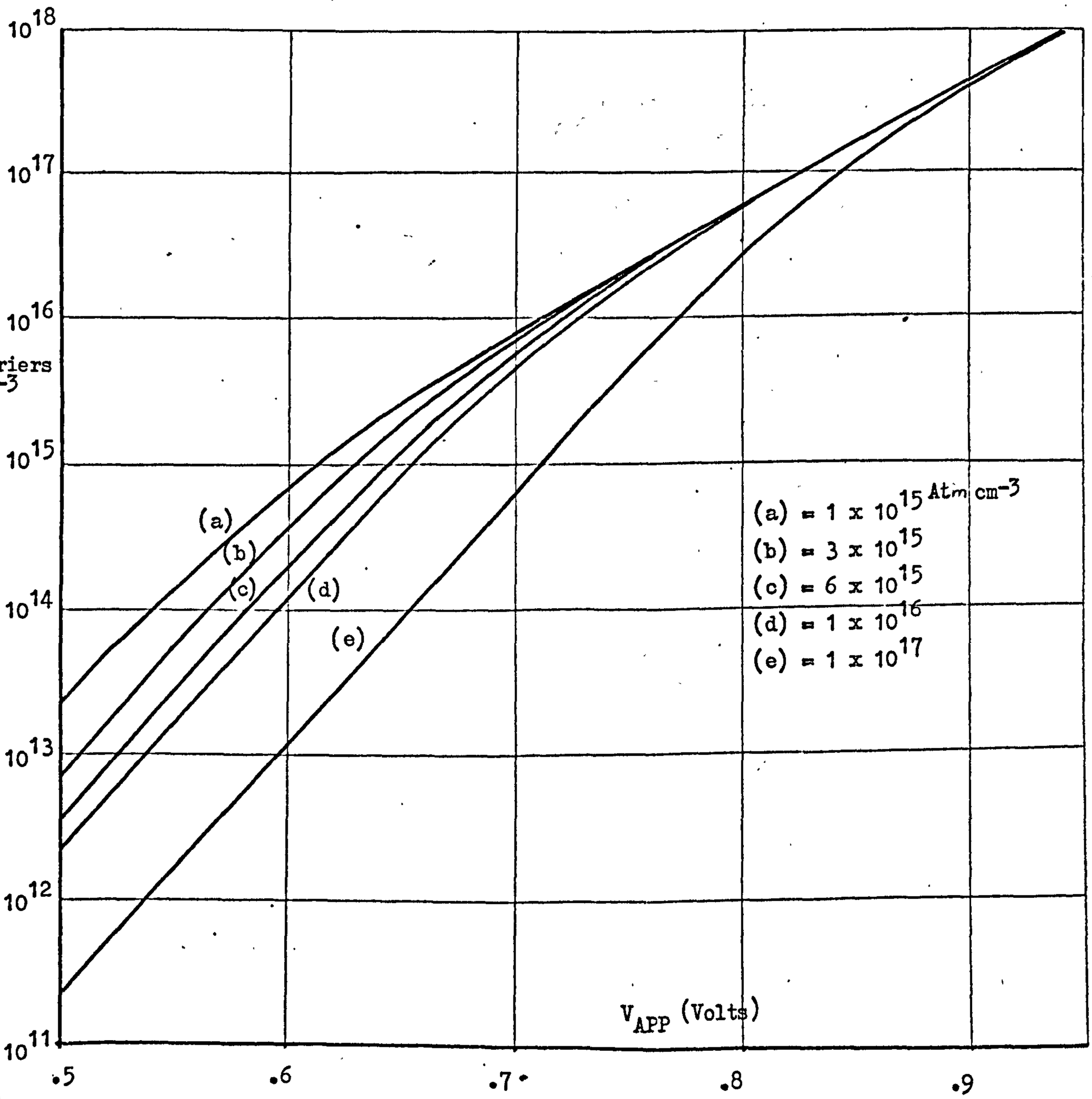


FIGURE 3.1

Potential distribution in the I^2L gate.

Figure 3.2.

Injected Carrier level v V_{APP} one sided junction, carriers at depletion region edge, 20°C



$$P_n = \frac{n_i^2}{N_{D_{EPI}}} \exp(qV_J/KT) \qquad (N_{D_{EPI}} = N_{EPI})$$

$n = P_n + N_{D_{EPI}}$ due to quasi neutrality

$$V_S = \frac{KT}{q} \ln \frac{P_n + N_{D_{EPI}}}{N_{D_{EPI}}}$$

Substituting $V_{APP} - V_S$ for V_J

$$p_n = \frac{n_i^2}{N_{D_{EPI}}} \exp\left(\left(V_{APP} - \frac{KT}{q} \ln\left(\frac{p_n + N_{D_{EPI}}}{N_{D_{EPI}}}\right)\right) q/KT\right)$$

$$p_n = \left(\frac{N_{D_{EPI}}^2}{4} + n_i^2 \exp(qV_{APP}/KT)\right)^{\frac{1}{2}} - \frac{N_{D_{EPI}}}{2} \qquad 3.1.$$

Equation 3.1. is used to describe minority carrier levels in the low doped epitaxy. Figure 3.2. shows injected carrier level plotted against applied bias with epitaxy doping as a parameter. The function is continuous between the low injection regions where

$$p_n = \frac{n_i^2}{N_{D_{EPI}}} \exp(qV_{APP}/kT) \text{ (from binomial expansion)} \qquad p_n \ll N_{D_{EPI}}$$

and the high injection regime where

$$p_n = n_i \exp(qV_{APP}/2KT) \qquad p_n \gg N_{D_{EPI}}$$

3.2.2. Hole Current into the epitaxial Buried N^+ structure

Let N, N^+ = epitaxial and buried N^+ dopings respectively.

W_E = width of epitaxial low doped region

D_E = minority carrier diffusion coefficient in epitaxy

τ_E = minority carrier life time in epitaxy

Minority carrier density in the Epitax-Buried N+ regions of the I^2L gate.

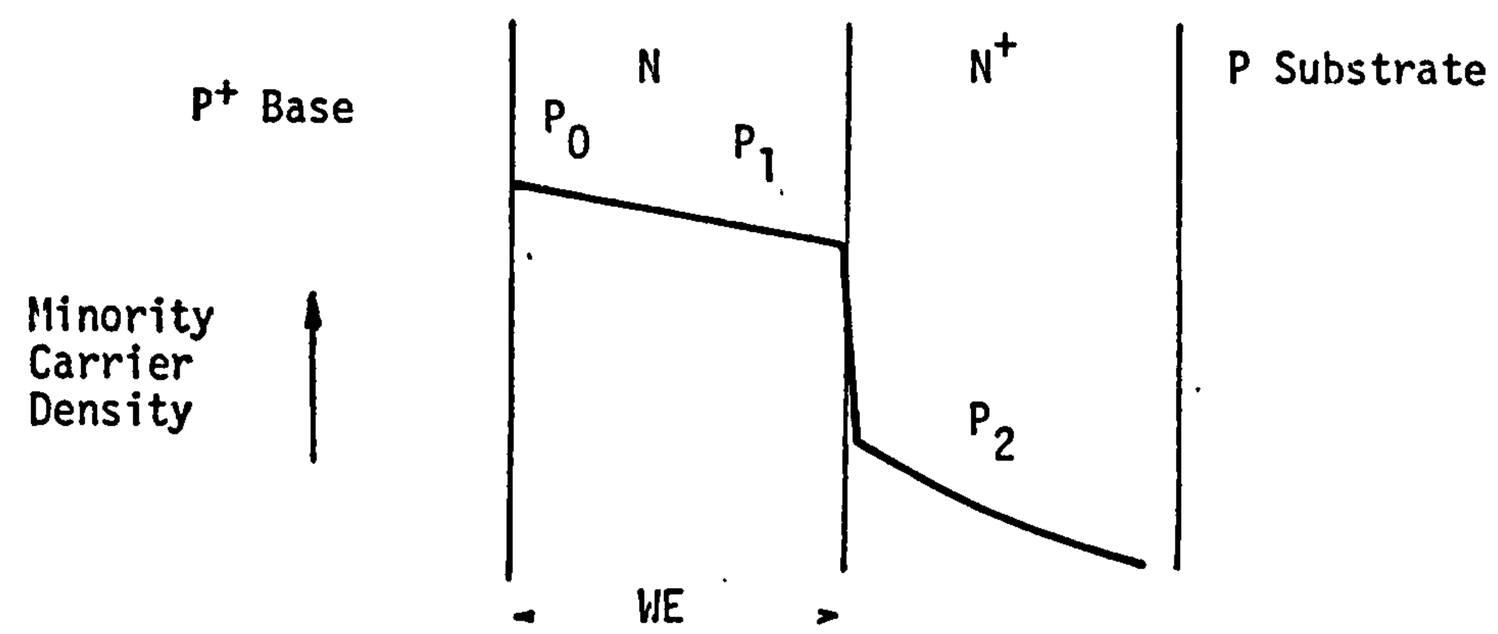


FIGURE 3.3

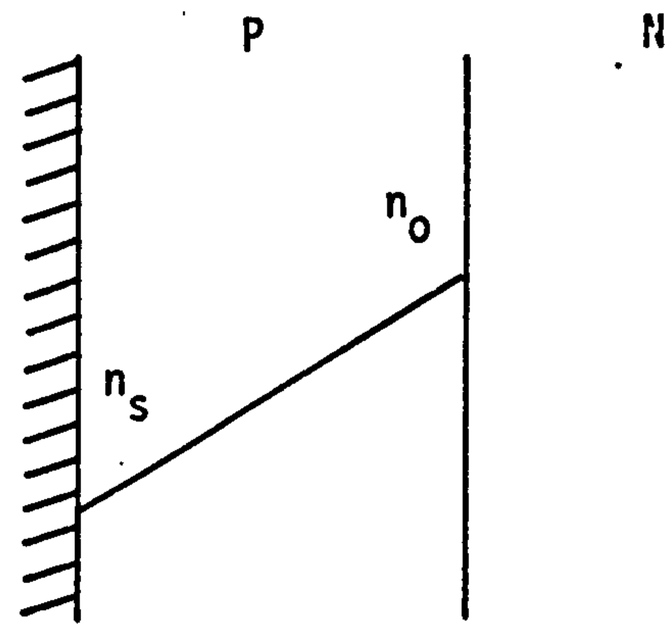


FIGURE 3.4(a)

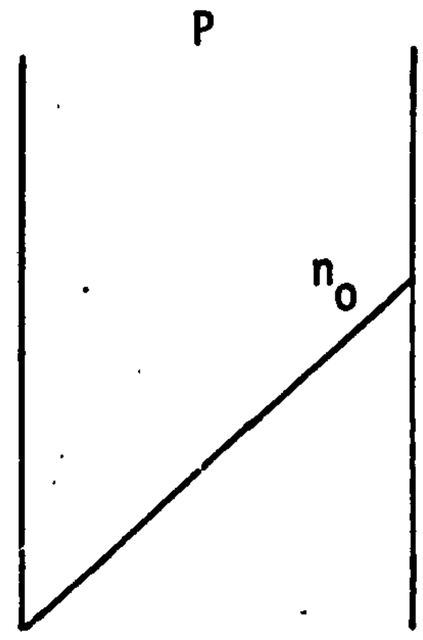


FIGURE 3.4(b)

Minority carrier densities in the extrinsic base regions of the I^2L gate.

L_E = minority carrier diffusion length in epitaxy = $\sqrt{D_E \tau_E}$

W^+ = width of buried N^+ region

D^+ = minority carrier diffusion coefficient in buried N^+

τ_+ = minority carrier lifetime in buried N^+

L^+ = minority carrier diffusion length in buried $N^+ = \sqrt{D^+ \tau^+}$

J_P = hole current flowing into epitaxy.

This analysis assumes that $L_E \gg W_E$
Figure 3.3. shows-

If $L_E \gg W_E$, then $J_P \simeq q (P_0 - P_1) \frac{D_E}{W_E}$ 3.2.

assuming field in epitaxy is negligible so that $J_p = q D \frac{dP}{dx}$

If the quasi-Fermi potential is constant across the buried N^+ epitaxial boundary, then

$$p_1 \cdot n_1 = n_i^2 \exp (q \psi / KT)$$

also $$p^+ = n_i^2 \exp (q \psi / KT)$$

Thus $$p_1 n_1 = p^+ \cdot N^+$$

$$p^+ = \frac{p_1 n_1}{N^+}$$

where p^+ and N^+ are the hole and electron concentrations respectively in the buried N^+ at epitaxial interface, p_1 and n_1 are hole electron concentrations in epitaxy at Buried N^+ interface. Assuming charge neutrality and low injection in the buried N^+

$$p^+ = \frac{p_1 (p_1 + N)}{N^+}$$

J_P can be represented as the sum of the recombination current in the epitaxy and the current transport into the buried N^+. Ignoring any recombination which may occur in the epitaxy-buried N^+ interface (see 20) which is small compared to other currents, we have

$$J_P = q\frac{(p_0 + p_1)}{2\tau_E} + q\frac{p^+ D^+}{L^+}\coth\frac{W^+}{L^+} \qquad 3.3.$$

[$(p_0 + p_1)/2 \simeq$ average epitax concentration.]

Transport into buried N^+ is the same as that for a long base diode (see 21). The buried N^+ P substrate junction is an infinite recombination interface,

Solving for p_1 gives (from 3.2. and 3.3.)

$$p_1 = -\frac{\left\{\frac{2L_E^2 + W_E^2}{2\tau_E W_E} + \frac{D^+N}{N^+X}\right\} + \sqrt{\left(\frac{2L_E^2 + W_E^2}{2\tau_E W_E} + \frac{D^+N}{N^+X}\right)^2 + \frac{4p_0D^+}{N^+X}\left(\frac{2L_E^2 - W_E^2}{2\tau_E W_E}\right)}}{\frac{2D^+}{N^+X}} \qquad 3.4.$$

where $$X = \frac{L^+}{\coth\frac{W^+}{L^+}}$$

$$J_P = q\frac{(p_0 - p_1)D}{W_E} \qquad \text{from} \quad 3.2.$$

$$p_0 = \left(\frac{N^2}{4} + n_1^2 e^{qV/KT}\right)^{\frac{1}{2}} - \frac{N}{2} \qquad \text{from} \quad 3.1.$$

(where $N = N_{D_{EPI}}$

Using the value of P_1 from equation 3.4. in 3.2, reasonable values of hole current injected into the epitaxy are obtained. Although the expression is an approximation it agreed essentially with experimental data. It is, however, necessary to modify it to include injection dependent lifetimes, mobilities, heavy doping effects and effects of majority carrier current (electrons crossing epitaxy to base regions).

These problems will be discussed subsequently.

It is found that most reasonable values of W_E, L_E, N, L^+ W^+ and N^+ result in $P_1 \simeq P_0$.

3.2.3. Electron Injection into base diffused regions.

The injection model described in Chapter 2 showed that the electron injection into base diffused regions had two components;*

(1) Injection J_{NC} under contact covered regions (Figure 3.4a).

(2) Injection J_{NO} under oxide covered regions (Figure 3.4b).

Injection under contact covered regions can be described by the long base diode expression assuming the contact is an infinite recombination interface. Let

X_j = base junction depth

N_A = base doping concentration

S_o = surface recombination velocity

D_n, γ_n, L_n Diffusion coefficient minority carrier lifetime and diffusion length respectively in base region

Then

$$J_{NC} = q \frac{n_i^2 D_n}{L_n} \exp(qV/KT). \coth \frac{x_j}{L_n} \qquad 3.5.$$

Using similar arguments to those developed for current flow in the epitax,

$$J_{NO} = qD_n \frac{(n_o - n_s)}{x_j} \qquad 3.6.$$

where J_{NO} = the sum of current due to recombination in base region and current due recombination at oxide interface. Using the Shockley Read Hall (22) model to describe recombination through an intermediate energy level, surface recombination is as follows. At the surface assume recombination centres are

(* assuming negligible recombination in the intrinsic base regions)

mid gap (such centres are the most effective) and hole and electron capture cross-sections are equal.

$$D_n \left.\frac{dn}{dx}\right|_{surface} = S_o \frac{p_s n_s - n_i^2}{n_s + p_s + 2n_i}$$

in low injection region

$$p_s \gg n_s$$

$$p_s n_s \gg n_i$$

$$p_s > n_i$$

$$\therefore D_n \left.\frac{dn}{dx}\right|_{surface} \simeq S_o n_s, \text{ and } \frac{n_s + n_o}{2} \simeq \text{average electron concentration}$$

$$J_{NO} = q \frac{(n_o + n_s)\, x_j}{.2\, \tau_n} + q\, S_o\, n_s \quad \text{(i.e. recomination in the bulk of the base plus surface recombination)} \quad 3.7.$$

Equating expressions 3.6. and 3.7., solving for n_s and substituting into expression 3.6. gives

$$J_{NO} = q \frac{D_n n_i^2}{x_j N_A} \exp(qV/KT) \frac{(2x_j^2 + 2S_o \tau_n x_j)}{(x_j^2 + 2L_n^2 + 2S_o \tau_n x_j)} \qquad 3.8.$$

As for the case of injection into epitaxy it is found that $n_s \leq n_o$ for most reasonable values of region parameters.

The foregoing treatment assumes low level injection conditions in the p base regions. Equation 3.1. gives the hole concentration p_n at the depletion region boundary in the epitaxy as a function of the applied bias.

$$p_o = \left(\frac{N_D^2}{4} + n_i^2 \exp\ qV_{APP}/KT\right)^{\frac{1}{2}} - \frac{N_D}{2}$$

$$n_n = p_o + N_D \text{ due to charge neutrality}$$

$$\therefore n_n = \left\{\frac{N_D^2}{4} + n_1^2\ e^{qV/KT}\right\}^{\frac{1}{2}} + \frac{N_D}{2}$$

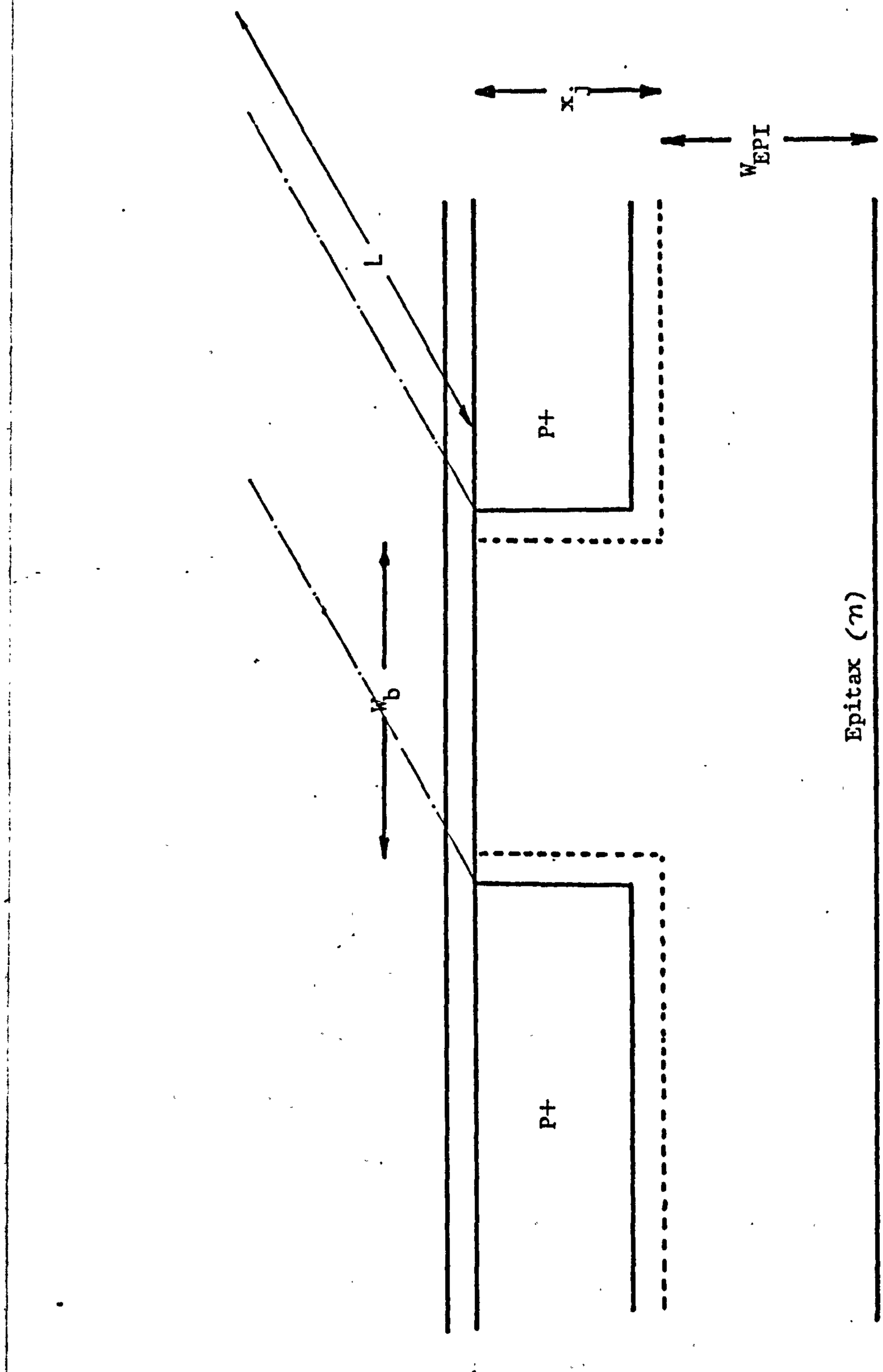


FIGURE 3.5 SIMPLE SCHEMATIC CROSS-SECTION LATERAL PNP

$$p_o \cdot n_n = n_i^2 \exp qV_{APP}/KT$$

As $$p_o \cdot n_n = p_p \cdot n_n$$

and $$P_p = N_A \text{ (low injection)}$$

then $$n_p = \frac{n_i^2}{N_A} \exp (qV_{APP}/KT)$$

The injected electron concentration in the oxide covered base regions maintains its dependence on qV_{APP}/KT when the epitaxy is in high injection, even though the junction voltage is reduced due to the field across the injected holes in the epitaxy. This arises because the electron concentration is increasing at the junction at a rate proportional to the junction voltage.

3.2.4. Lateral re-injection current

The injector transistor is a lateral pnp type and this type of structure has been extensively investigated (23,24). Figure 3.5. shows a simple schematic of a lateral pnp with junction depth, and layer widths and depletion regions indicated. The figure shows no radius of curvature on the p diffused regions. The p-dopant will diffuse laterally under the passivating oxide at the photoengraved window edge in the real case. For the limiting case when the epitaxial width is zero the lateral reinjection current is:

$$I_L = \frac{qn_i^2 D}{N_D W_b} \exp (qV/KT)\, x_j L$$

(i.e. the collector current of a lateral transistor).

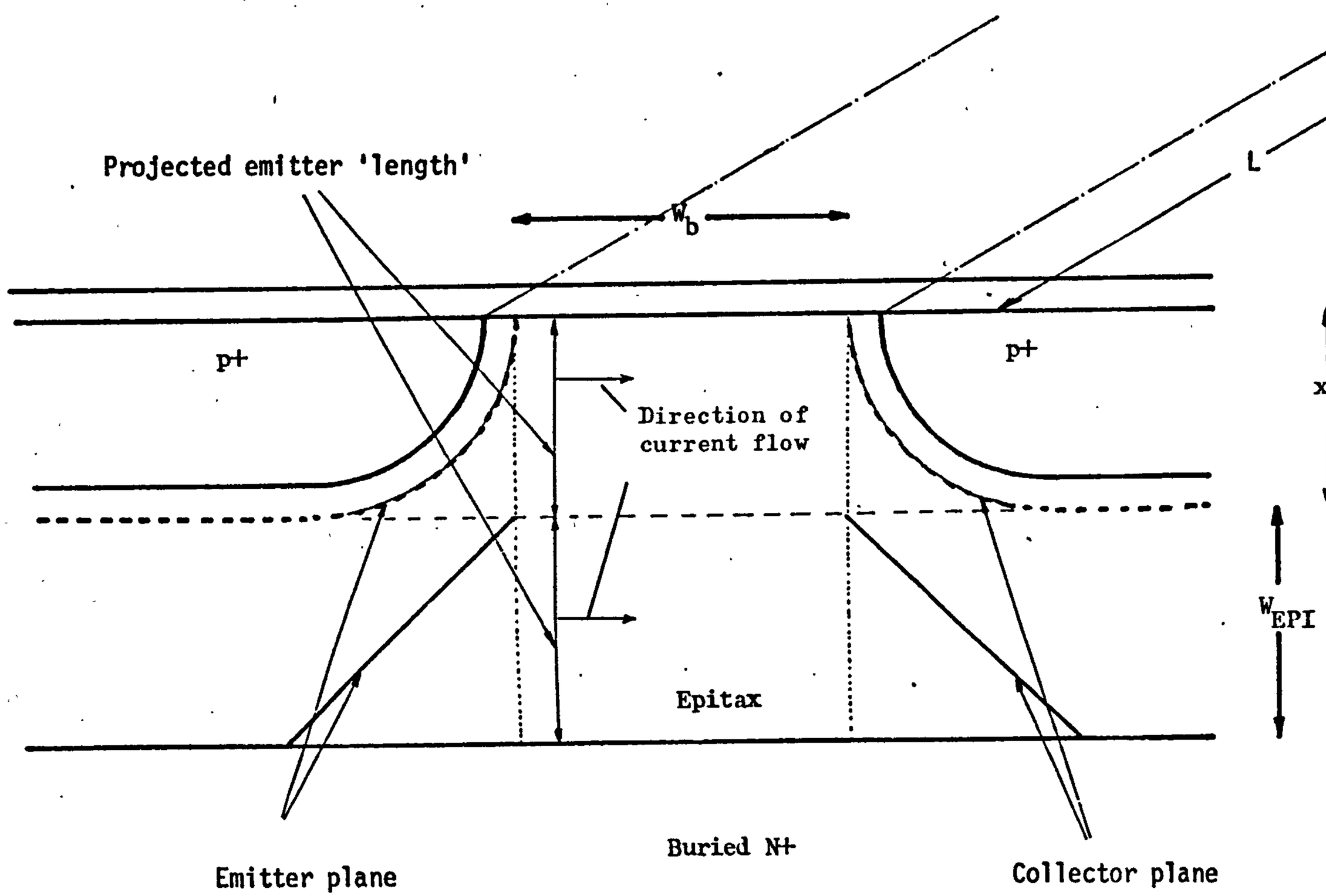


FIGURE 3.6

SCHEMATIC CROSS-SECTION LATERAL pnp

In the real device as shown in Figure 3.6. the lateral carrier flux is not one dimensional because current flow in the epitaxial region becomes significant as soon as W_{EP1} is non-zero. The nature of the current flow in the epitaxy was first investigated by Fulkerson (23). Sunlin Chou (24) introduced a function F_{GC} which related the non-uniform base width and epitaxy thickness to the collector current.

$$I_L = \frac{qn_i^2 D_P}{N_D W_b} \quad (\exp qv/KT)\, x_j L \quad F_{GC} \qquad 3.8.$$

Chou determined F_{GC} using a two dimensional computer analysis. However an approximate value of F_{GC} can be determined by analysis of the lateral's structure in two parts as follows:

a) Assuming radial diffusion at the photoengraved window edge, the area between collector and emitter of the lateral transistor contained within the p region junction depth is :

$$W_b\, x_j + 2\, x_j^2 - \frac{\pi}{2} x_j^2$$

If emission of the minority carriers takes place up to a depth x_j below the surface then the effective base width is defined as:

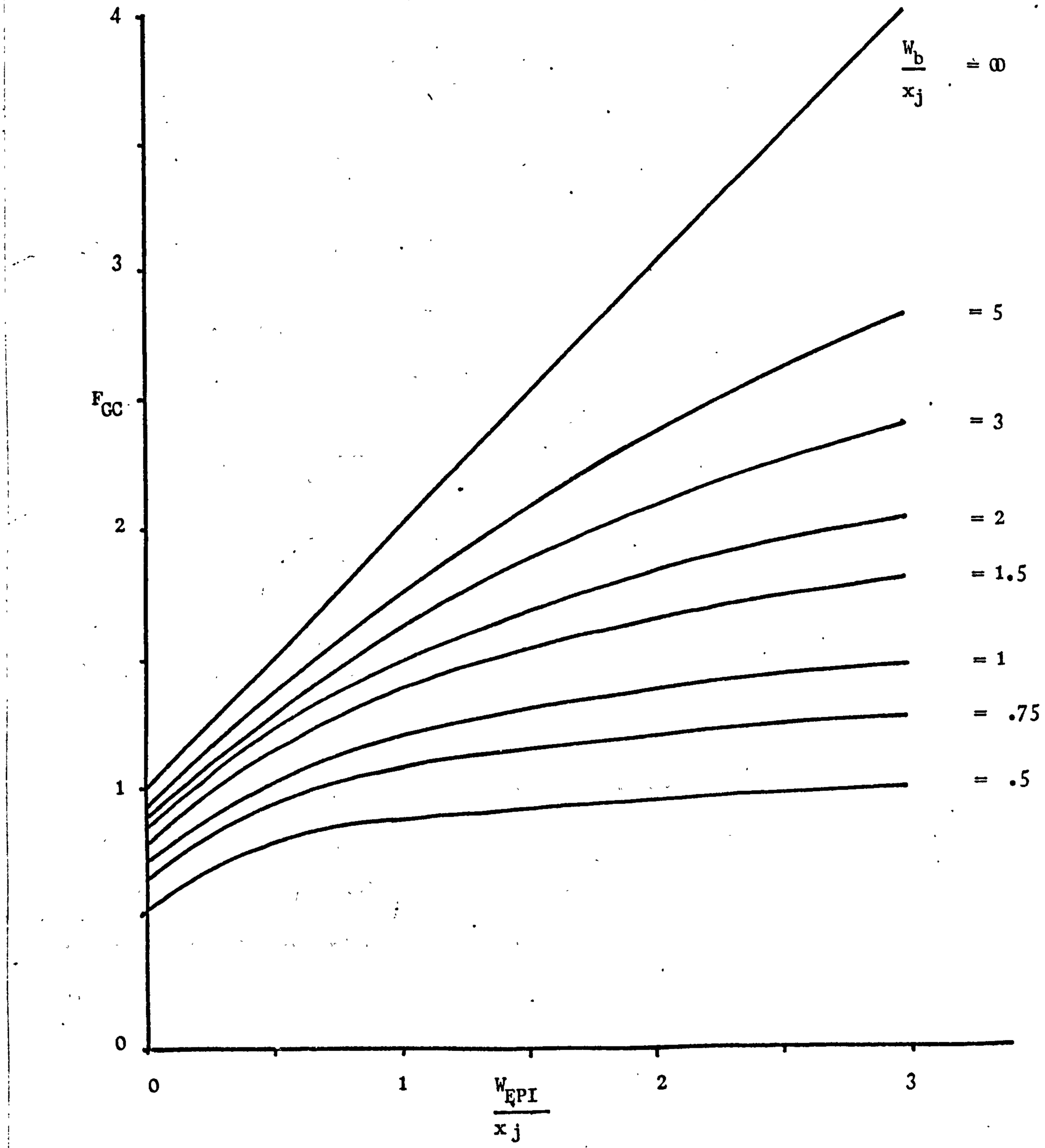
$$W_b\,(\text{eff}) = \frac{\text{Area of plane of cross-section of base region between emitter and collector planes}}{\text{Projected length of intersection of emitter plane with above plane in direction of current flow.}}$$

$$= W_b + x_j\,(2 - \frac{\pi}{2})$$

b) As was shown in section 3.2.2. the minority carrier level is nearly uniform under the P emitter between its depletion

FIGURE 3.7

APPROXIMATE 2-DIMENSIONAL CORRECTION FACTOR FOR LATERAL pnp (F_{GC})



region and the epitaxial buried N^+ interface. This excess of minority carriers will result in a diffusion gradient of carriers from under the emitter, to the region under the collector, where they will be collected. If this emission and collection is considered to occur from a boundary line under the p-diffusion as shown in Figure 3.6. then the effective base width of this region (if the emission depth is W_{EPI},) becomes : —

$$W_b + W_{EPI}$$

Thus $I_L = \frac{qn_i^2}{N_D} D_p \exp(qV/KT) L \left(\frac{x_j}{W_b + x_j(2-\frac{\pi}{2})} + \frac{W_{EPI}}{W_b + W_{EPI}}\right)$

by summation of the currents in the two parts of the transistor and comparing with equation 3.8. results in:

$$F_{GC} = \left(\frac{W_b}{W_b + x_j(2-\frac{\pi}{2})} + \frac{W_{EPI}\, W_b}{x_j\,(W_b + W_{EPI})}\right)$$

F_{GC} is shown plotted against Figure 3.7.

The $\frac{n_i^2}{N_D} \exp(qV/KT)$ term should be substituted with the expression

$$P = \left(\frac{N_D^2}{4} + n_i^2 \exp(qV/KT)\right)^{\frac{1}{2}} - \frac{N_D}{2}$$

(equation 3.1.)

(Injection in both high and low injection regimes)

Also in high level injection the effective minority carrier diffusion coefficient for a collector current is enhanced due to the creation of a potential gradient down the minority carrier profile.

$$J_L = q\mu_p \; p\,E - qD_p \frac{dp}{dx} \quad (J_L \text{ Lateral re-injection current density})$$

$$J_n = q\mu_n \; n\,E + qD_n \frac{dn}{dx}$$

Where J_n is the current due to electron transport across the base.

for the case considered $J_\eta \rightarrow 0$, therefore

$$q\mu_n \; nE = qD_n \frac{dn}{dx} \qquad D_n = \frac{KT}{q}\mu_n \text{ (Einstein relation)}$$

$$E = -\frac{KT}{q} \; \frac{1}{n} \; \frac{dn}{dx}$$

assuming $\frac{dn}{dx} = \frac{dp}{dx}$

and $n = p + N_D$

$$E = \frac{-KT}{q} \; \frac{1}{p + N_D} \; \frac{dp}{dx}$$

substituting for E in equation for hole current .

$$J_L = q\mu_p \; p\left(\frac{-KT}{q} \; \frac{1}{p + N_D} \cdot \frac{dp}{dx}\right) - qD_P \; \frac{dp}{dx}$$

$$= q\left(D_p \frac{p}{p + N_D} \; \frac{dP}{dx} + D_p \; \frac{dP}{dx}\right)$$

$$J_L = -qD_p \; \frac{dP}{dx} \; \left(\frac{2p + N_D}{p + N_D}\right)$$

When $p \leqslant N_D$

$$J_L = -qD_P \; \frac{dP}{dx}$$

As injection increase to case where $p \gg N_D$

$$J_L = -qD_P \; \frac{dP}{dx} \cdot 2$$

The base current component of the upward npn due to the reinjection caused by pnp saturation is then

$$I_L = \frac{qp\,Dp}{W_b} \left(\frac{2p + N_D}{p + N_D}\right) x_j \, L \cdot F_{GC}$$

where $p = \left(\frac{N_D^2}{4} + n_i^2 \exp (qV/KT)^{\frac{1}{2}} - \frac{N_D}{2}\right)$ 3.1.

and $F_{GC} = \frac{W_b}{W_b + x_j(2 - \frac{\pi}{2})} + \frac{W_{EPI}\ W_b}{x_j(W_b + W_{EPI})}$ 3.9.

3.2.5. Depletion Region Recombination

The upward I^2L npn transistor in comparison to the downward operated device has a large emitter junction area and a large junction perimeter. These geometric factors severely degrade the low current gain performance, and as a result increase the value of the lowest power at which the gate will operate. The depletion region recombination current associated with the emitter area is

$$I_{rec} = qA_J \int_0^{W_D} U dx$$

A_J is junction area, W_D is depletion layer width, U is the depletion region recombination rate.

For the case to be considered assume single level traps, equal hole and electron capture cross-sections, and thermal velocities. From Shockley Read Hall (22).

$$U = 6\ V_{th}\ N_t \frac{pn - n_i^2}{n+p + 2ni \cosh(\frac{E_t - E_i}{KT})}$$

As most effective traps are near energy E_i

$$U = 6\ V_{th}\ N_t \frac{p_n - n_i^2}{n+p + 2ni}$$

substituting $\tau = 1/(6\ V_{th}\ N_t)$

Where τ is low injection minority carrier lifetime.

$$U = \frac{1}{\tau} \frac{pn - n_i^2}{p+n + 2n_i}$$

6 = capture cross-section of electrons and holes
Vth = carrier thermal velocities
N_t = density of recombination centres.

$$pn = n_i^2 \exp(qV/KT)$$

$$U = \frac{1}{\tau} \cdot \frac{n_i^2(\exp(qV/KT) - 1)}{n+p + 2n_i} \qquad 3.10.$$

For a given forward bias U is maximised when the denominator in equation 3.10. is minimised, n_i is effectively a constant and product n p is constant. For minimum $d(p + n) = 0$

$$dp = -dn = pn \frac{dP}{p^2}$$

$$p = n$$

This condition exists at the position in the depletion layer where the intrinsic Fermi level is mid-way between the hole and electron quasi Fermi levels.

$$p = n = n_i \exp(qV/2KT)$$

Substitution into 3.10, gives maximum recombination rate as

$$U_{max} = \frac{1}{\tau} \frac{n_i(\exp(qV/KT) - 1)}{2(\exp(qV/2KT) + 1)}$$

If

$$V \gg \frac{KT}{q}$$

$$I_{max} \simeq \frac{1}{2} \tau n_i \exp(qV/2KT)$$

Approximating the recombination rate in the depletion layer by U_{max} gives

$$I_{rec} = \frac{1}{2} q \frac{n_i}{\tau} W \exp(qV/2KT) A_J$$

as the recombination current in depletion region where

W = depletion layer width

A_J = junction area.

3.2.6. Surface Depletion Region Recombination

Using similar arguments to those for the area term, the surface (i.e. where depletion region intersects silicon-silicon dioxide interface) depletion region recombination can be written as

$$I_{SR} = \frac{1}{2} q S n_i W \exp(qV/2KT) P$$

S = surface recombination in depletion layer

W = depletion layer width

P = junction perimeter

Experimentally it is found that the surface depletion region recombination is many orders of magnitude larger than the area depletion region recombination. (see Appendix 1). Thus in injection analysis the area terms will be omitted.

3.3. EXTENSIONS TO THEORETICAL CONSIDERATIONS

The previously presented analyses form the bases of the understanding of the I^2L device. However, certain parts of the analysis need modifying to include the following specific effects not included in these basic observations.

3.3.1. The Effect of Injection Level on Recombination

The models proposed for the epitaxial and base surface recombination assume a single level Shockley Read Hall (22) mechanism. In low injection this is correct.

$$U \simeq \frac{P}{\tau}$$

U is recombination rate, P is excess carrier concentration and τ is characteristic lifetime. In general

(

$$U = \frac{\sigma_p \sigma_n V_{th} N_T (p_n - n_i^2)}{\sigma_n (n + n_i \exp(E_t - E_i)/KT) + \sigma_p (p + n_i \exp(E_i - E_t)/KT)}$$

σ_p, σ_n = hole and electron capture cross-sections

V_{th} = thermal velocity

N_t = concentration of recombination centres

E_t = energy level of recombination centre in band gap.

Two simplifying assumptions will be made in order to produce a manageable solution, hole and electron capture cross-sections will be assumed equal, and the energy level of the recombination centre is assumed to be mid gap, i.e. $E_t = E_i$. This assumption maximises U.

Hence $$U = \frac{\sigma V_{th} N_T (P_n - n_i^2)}{p + n + 2n_i}$$

which gives $$\sigma V_{th} N_t = \frac{1}{\tau}$$

$$U = \frac{1}{\tau} \frac{pn - n_i^2}{p + n + 2n_i}$$

For cases under consideration, terms in n_i are ignored as they are small in comparison to the others.

$$U = \frac{1}{\tau} \frac{pn}{p+n}$$

Using equation 3.1. and invoking charge neutrality, the recombination rate in the epitaxial region of the I^2L device becomes

$$U = \frac{1}{\tau} \frac{n_i^2 \exp(qV/KT)}{2(N_D^2/4 + n_i^2 \exp(qV/KT))^{\frac{1}{2}}} \qquad 3.11.$$

$$p = (N_D^2/4 + n_i^2 \exp(qV/KT))^{\frac{1}{2}} - N_D/2 \qquad 3.1.$$

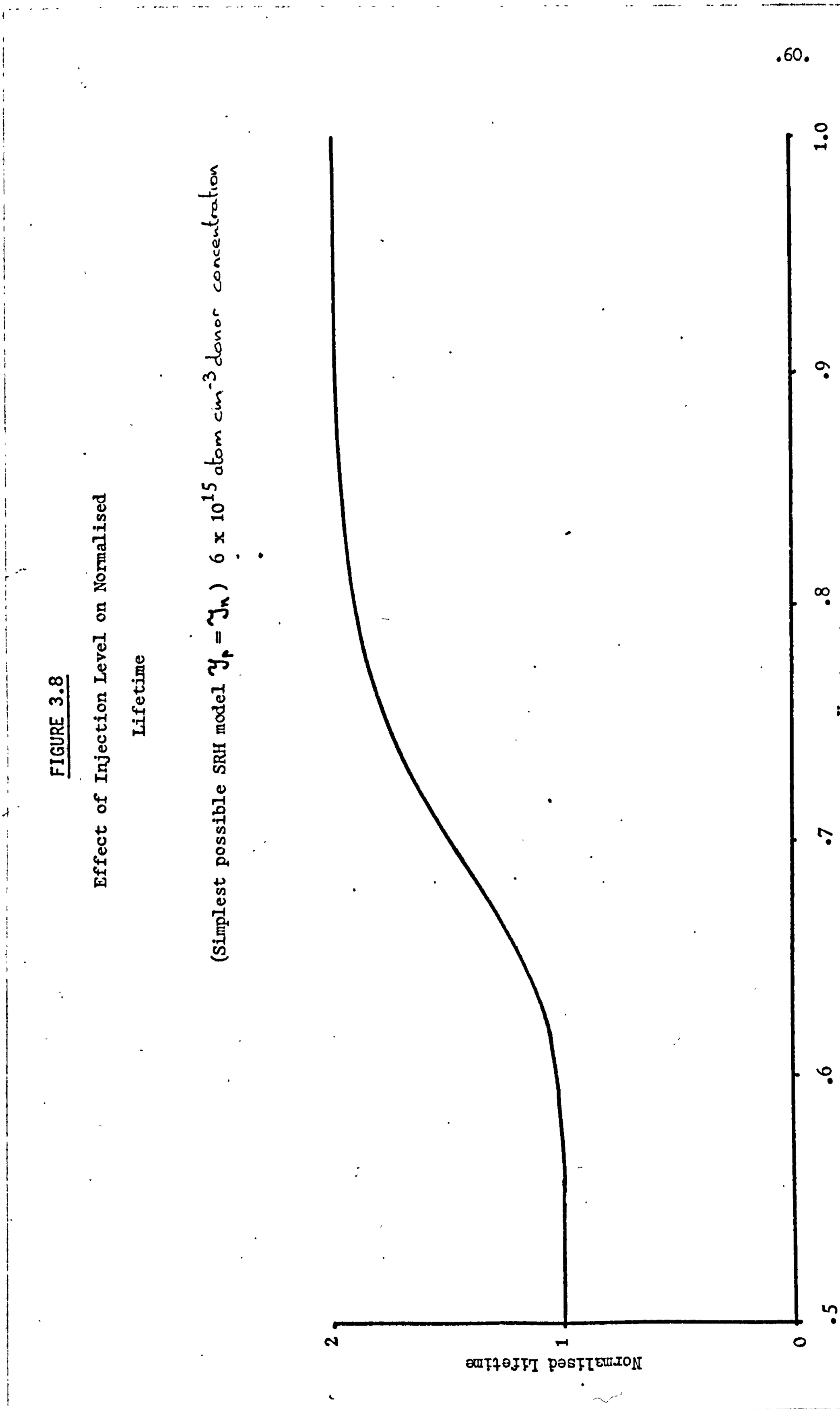


FIGURE 3.8

Effect of Injection Level on Normalised Lifetime

$$n = (N_D^2/4 + n_i^2 \exp(qv/KT))^{\frac{1}{2}} + N_D/2$$

In the low injection approximation $P < n$

Then $$U = \frac{P}{\tau}$$

In order to be corrected for injection level τ must be modified by some factor, thus

$$U = \frac{P}{\tau R}$$

From equation 3.11.

$$R = \frac{2((N_D^2/4 + n_i^2 \exp(qV/KT))^{\frac{1}{2}} - N/2)\ (N_D^2/4 + n_i^2 \exp(qV/KT))^{\frac{1}{2}}}{n_i^2 \exp(qV/KT)}$$

Figure 3.8. shows R as a function of V_{be} for $N_D = 6 \times 10^{15}$ At cm^{-3}. From low injection to high injection for this case U halves, or it could be considered that τ doubles. It should be pointed out that this particular solution is only the simplest possible and the recombination parameters are likely to be much more complicated in real devices.

3.3.2. The effect of injection level and majority carrier currents on effective diffusion coefficients in epitaxy.

Implicit in the derivations for equation 3.4. (injected current into epitaxy plus buried N^+) is that there is no field in the epitaxial region of the I^2L device. This is not necessarily so, however, a rigorous analytic solution to this problem is unfortunately not obtainable. Hertlett (25) has derived a solution for the field distribution in the low doped region of a P^+NN^+ diode, unfortunately this solution cannot be transferred to the I^2L case. Chou (17) has developed a computer aided

analysis of the low doped region of a P^+NN^+ diode and quantitative information is obtainable for this source, although care is necessary for correct interpretation.

This injection model of current flow into the epitaxy ignored the effect of the electron current transversing the epitaxy in order to maintain the injections into the base diffused regions. To describe the gross behaviour of the field in the epitaxy, let

$$J_n = a\, J_p$$

that is electron and hole currents in a given element of the device are related by factor 'a' and J_n and J_p are constant across epitaxy.

$$J_n = q\,\mu_n E n + q\, D_n \frac{dn}{dx}$$

$$J_p = q\,\mu_p E p - q\, D_p \frac{dp}{dx}$$

Invoking charge neutrality and making the assumption that hole and electron gradients are equal

$$J_n = q\,\mu_n E\,(p + N_D) + q\, D_n \frac{dp}{dx}$$

$$J_p = q\,\mu_p E p - q\, D_p \frac{dp}{dx}$$

$$\mu_p \simeq 2.5\,\mu_n$$

and Einstein relationship

$$D = \frac{KT}{q}\mu$$

$$E = \frac{KT}{q}\,\frac{dp}{dx}\,\frac{(2.5\mu_p + a\mu_p)}{p\,a\mu_p - 2.5\mu_p(p+N_D)}$$

$$J_p = q\, Dp\, \frac{dp}{dx}\,\frac{(5p + 2.5N_D)}{((a-2.5)p - 2.5N_D)}$$

FIGURE 3.9(a)

Normalised Diffusion Coefficient.

v Base Emitter Bias.

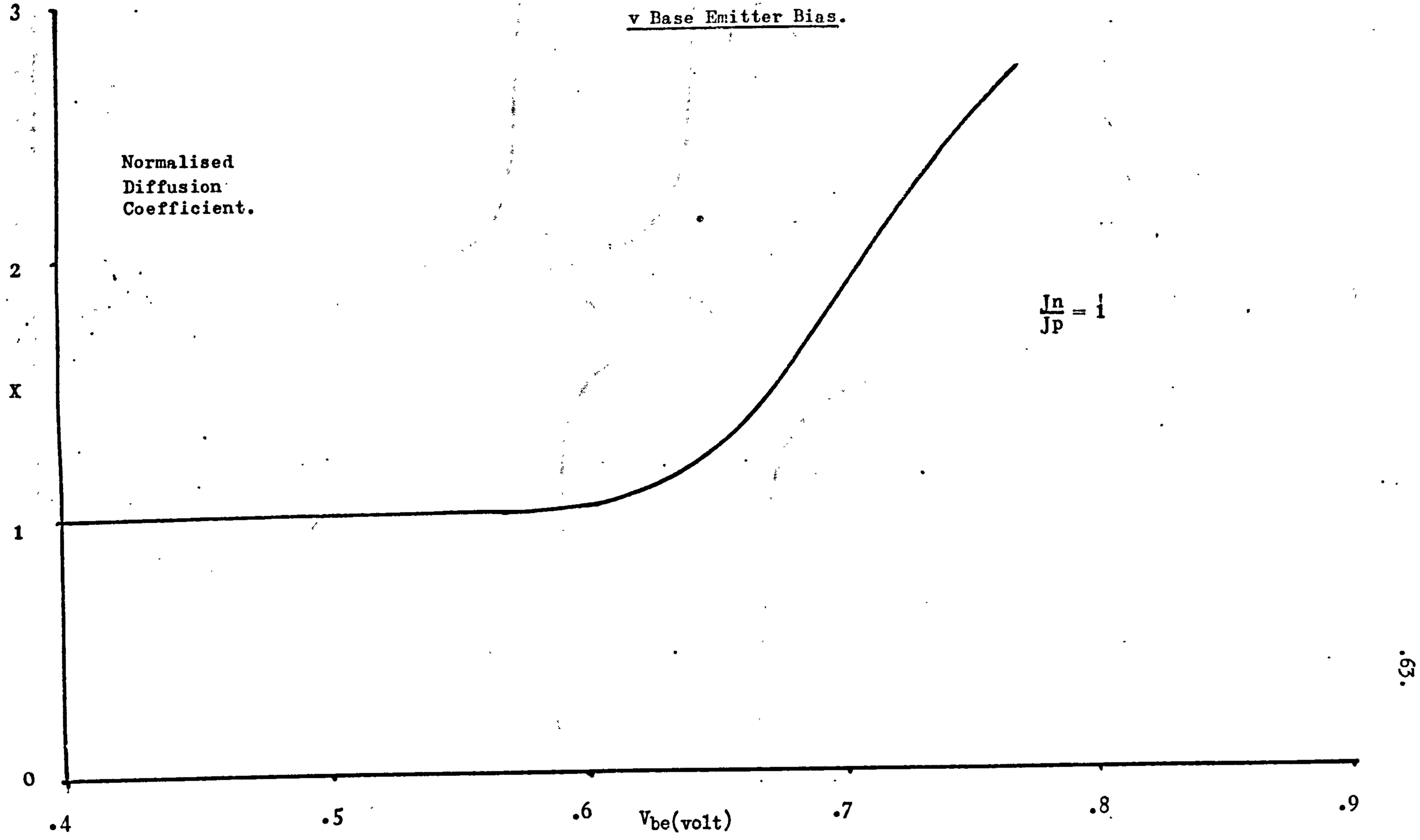
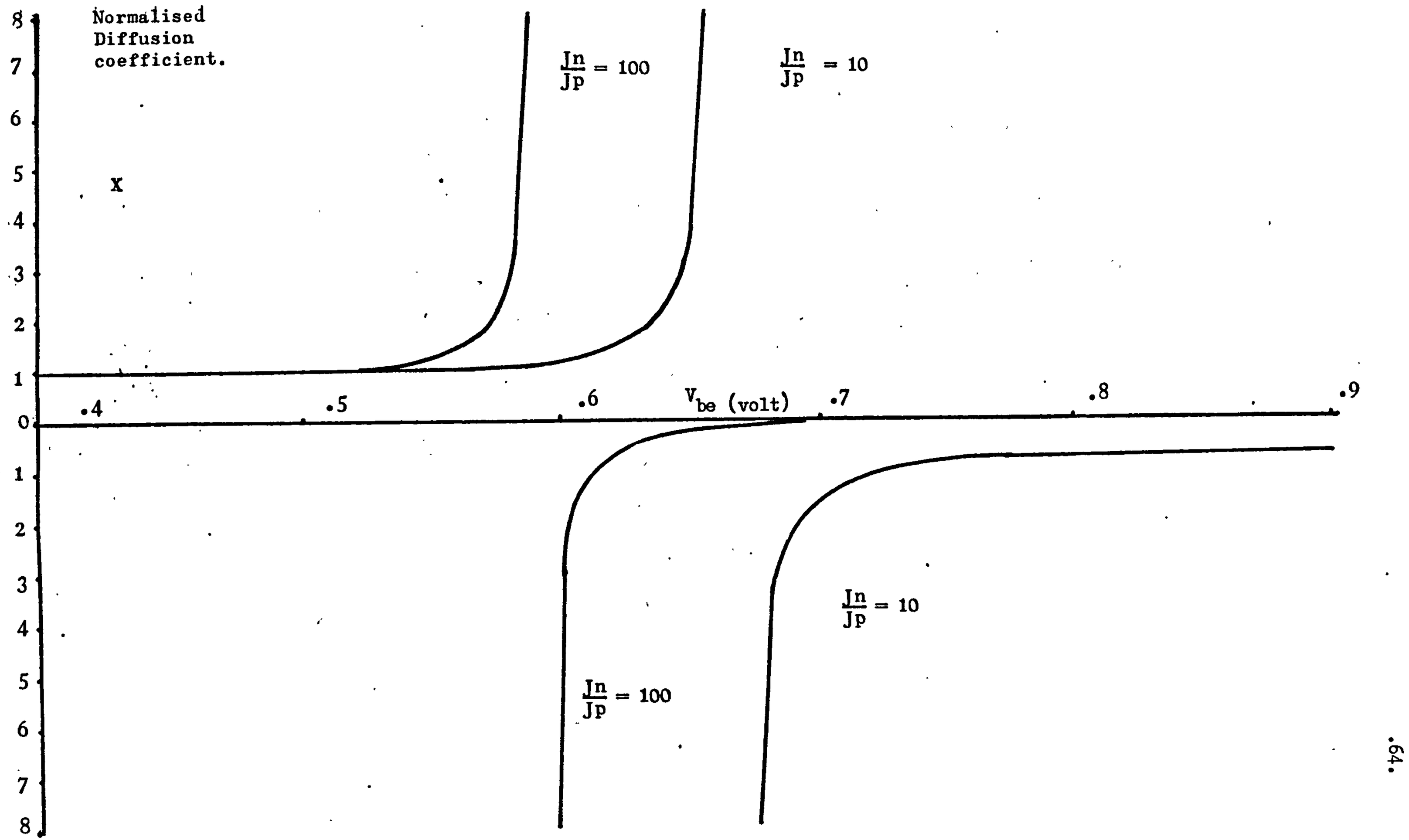


FIGURE 3.9(b)

Normalised Diffusion Coefficient v Base Emitter Bias.



The function $X = \frac{5p + 2.5N_D}{(a-2.5)p-2.5N_D}$

is shown in Figures 3.9a, b for 'a' = 1, 10, and 100.

The case 'a' = 1 corresponds to the regions of the device covered by base oxide. The case 'a' = 100 corresponds to the region under a collector. In oxide covered regions the epitaxial field results in a gradual increase in effective diffusion coefficient with injection, whilst under collectors there is an apparent changing of the sign of the hole gradient with increased injection. This result has been partially confirmed by a Gummel Poon type model (26) of the I^2L gate in which a = 10. The hole gradient changed sign near the buried N^+ interface as injection increased. Values of 'a' greater than 10 resulted in the model failing to converge at biases needed to observe the effect.

Although the hole gradient changes sign in the epitaxy under the collector, the hole current flow is still in the same sense as volume recombination and buried N^+ recombination will only be changed in detail. The significance of this change in sign is most manifest on the upward collector current. In effect the base region under the collector has been swept out to the buried N^+ interface.

3.3.3. Injection Effects on diffusion coefficient and mobility-intercarrier scattering.

Chou (17) has shown that the assumption of constant mobility with changing injection level is unable to explain the behaviour of a P^+NN^+ diode. Fletcher (18) in an early publication,

suggested that the well known impurity (coulombic) and lattice (phonon) scattering mechanisms were inadequate to describe the mobility of minority carriers, and that effects due to carrier collisions should be included in mobility calculations.

Adopting a similar nomenclature to Chou (17) mobility is described by the following:

μ_L = lattice scattering component of mobility

μ_I = impurity scattering component of mobility

μ_{np} = intercarrier scattering component of mobility

$$\mu = (\mu_L^{-1} + \mu_I^{-1} + \mu_{np}^{-1})^{-1}$$

μ_L is obtained from the experimental data (27). For μ_I, there are two possible treatments:

(1) Rutherford scattering treatment by Conwell and Weisskopf (28).

(2) Quantum mechanical treatment of Brooks (29).

Agreement between these two results is close, and as the treatment by Conwell and Weisskopf is easier for calculation purposes this has been adopted as an expedient.

For μ_{np} the expression of Gummel and Scharfetter is used (30).

We have therefore:-

$$\mu_{Ln} = 2.1 \times 10^9 \, T^{-2.5} \ cm^2/V.s.$$

$$\mu_{Lp} = 2.3 \times 10^9 \, T^{-2.7} \ cm^2/V.s.$$

$$\mu_I = \sqrt{\frac{2}{\pi}} \cdot \frac{2\pi \epsilon^2 (KT)^{3/2}}{q^3 m^{*1/2} N_I \ln\left\{1 + \left(\frac{28\sqrt{\pi}\,\epsilon\, K T}{q^2 N_I^{1/3}}\right)^2\right\}} \ cm^2/V.s.$$

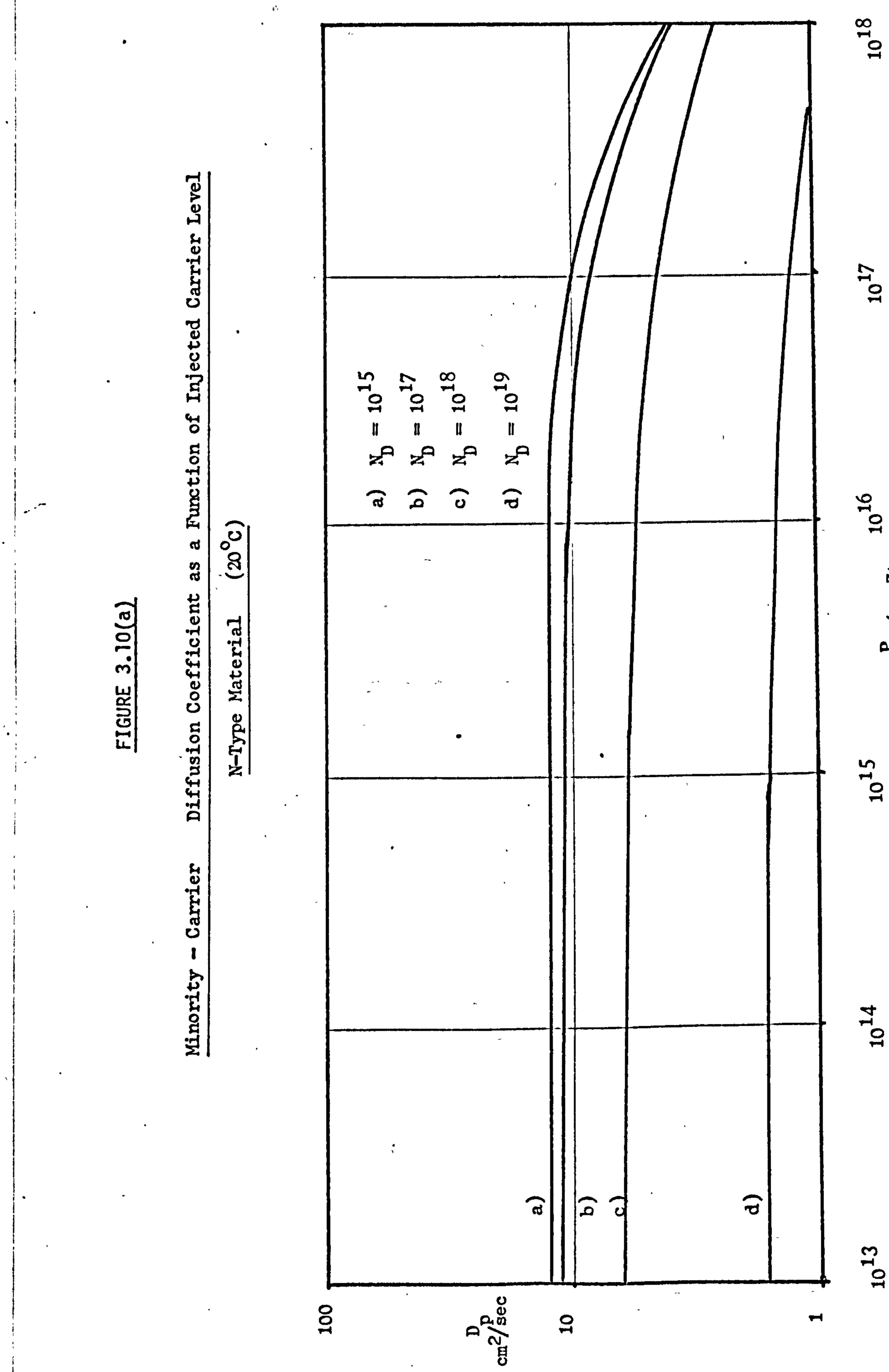
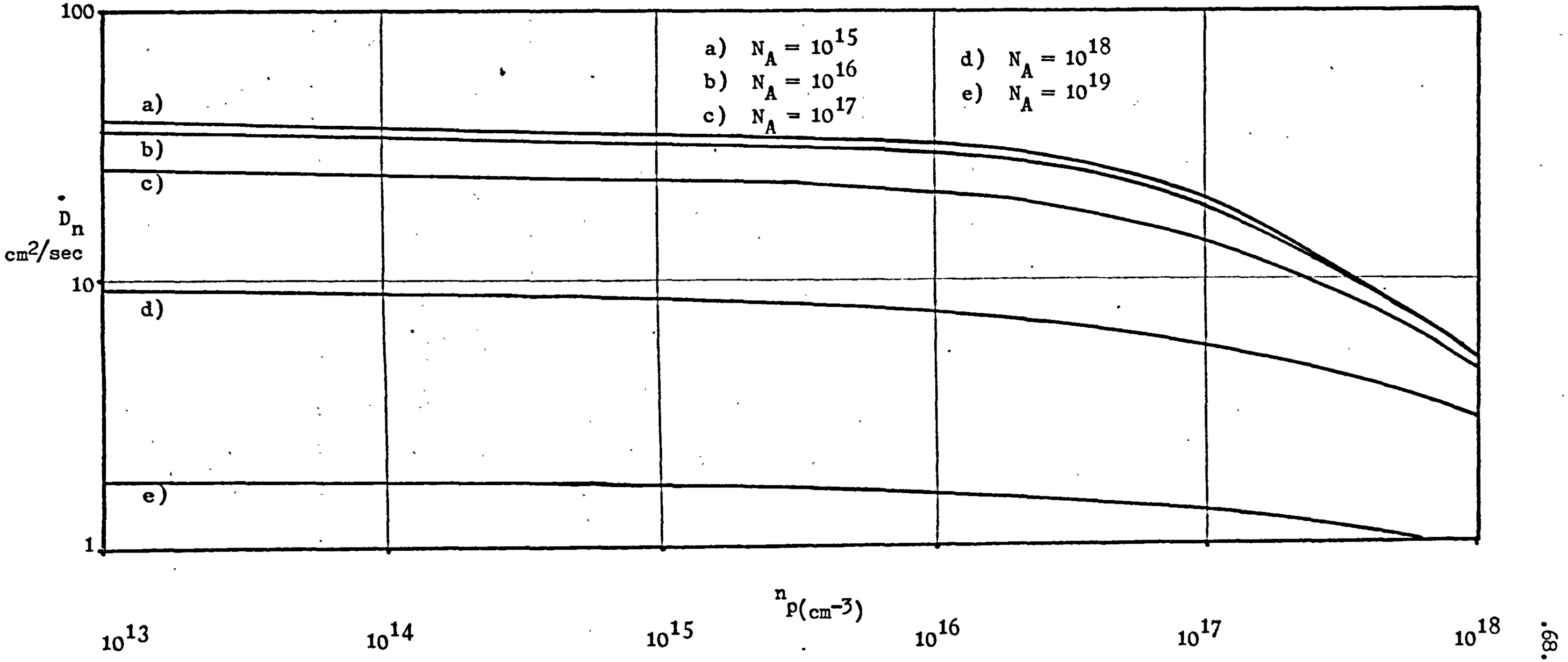

Minority - Carrier Diffusion Coefficient as a Function of Injected Carrier Level
N-Type Material (20°C)
a) $N_D = 10^{15}$
b) $N_D = 10^{17}$
c) $N_D = 10^{18}$
d) $N_D = 10^{19}$
D_p cm^2/sec
100
10
1
10^{13}
10^{14}
10^{15}
10^{16}
10^{17}
10^{18}
P_n (cm^{-3})

FIGURE 3.10(a)

FIGURE 3.10(b)

Minority Carrier Diffusion Coefficient as a Function of Injected Carrier Level P-Type Material (20°C)



$$\mu_{np} = 2 \times 10^{17}\, T^{3}/2 \left\{(np)^{\frac{1}{2}}.\ \ln(1 + 8.28\times10^{8}\, T^{2}(np)^{-1/3}\right\}^{-1} cm^{2}/V.s.$$

Figures 3.10. show the effect of impurity level and injection level upon minority carrier diffusion coefficient. This result shows the dramatic effect intercarrier scattering has on diffusion coefficient for low doped regions. Even under moderate injection, diffusion currents will be seriously modified.

3.3.4. Effect of finite base resistance on the I^2L gate

The base current of the I^2L device is supplied to one end of the base land. As base current is increased this results in a progressive debiassing of the base towards that part most remote from the injector. Figure 3.11. shows a simple equivalent circuit representation of a four collector I^2L gate. Using this sort of scheme, representing the base as a distributed resistance with suitable distributed loss diodes to represent the base current, an accurate representation of the multicollector I^2L gate is possible. In the solutions tried in this work it was found necessary to increase the number of points in the distributed network near to the injector; this is because this is the region of most rapidly changing bias.

A consequence of the debiasing of the base land is that the collector nearest the injector has a gain β_u which can increase rapidly at high base currents whilst the remote collector gain falls rapidly as it is deprived of most of its base drive current.

A consequence of this debiasing, which is analogous to current crowding in downward transistors, is that at high

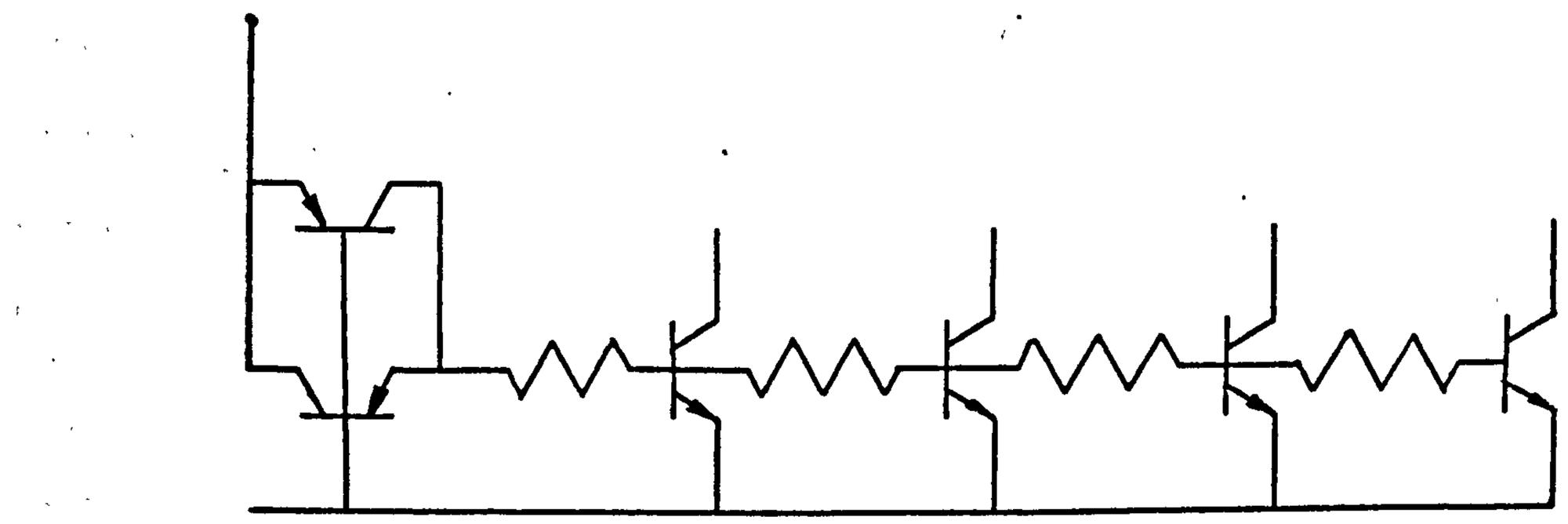


Figure 3.11

Simple equivalent circuit of 4-collector I^2L gate.

current most of the active charge, i.e. that charge associated with injection, is stored in that part of the device nearest the injector.

3.3.5. Heavy doping effects on band-gap narrowing

Implicit in most calculations of minority carrier injection levels are the assumptions of:-

(1) Non degeneracy

(2) Validity of Boltzmann statistics.

Both these assumptions are questionable in relationship to the higher doped regions of the I^2L gate. The consequence of ignoring the effect of these approximations is that the magnitude of current flow into those regions in which the approximations are not valid can be several orders of magnitude too large.

The effects of heavy doping have been studied by several authors, 31, 32, 33. The conclusion from the published work is that as doping is increased, discrete impurity levels in the energy gap are replaced by a continuous energy band, This results in a narrowing of the band gap. (Figure 3.12). This reduction of the band gap causes an increase in the minority carrier concentrations, which corresponds to an effective reduction in doping density. Calculations have been made by the author using an approximation to the relationships presented by Mock and van Overstraten, and the experimental treatment of Slotboom and De Graaf (32, 33). This treatment is used to calculate minority carrier levels using an effective intrinsic carrier concentration as a function of doping level.

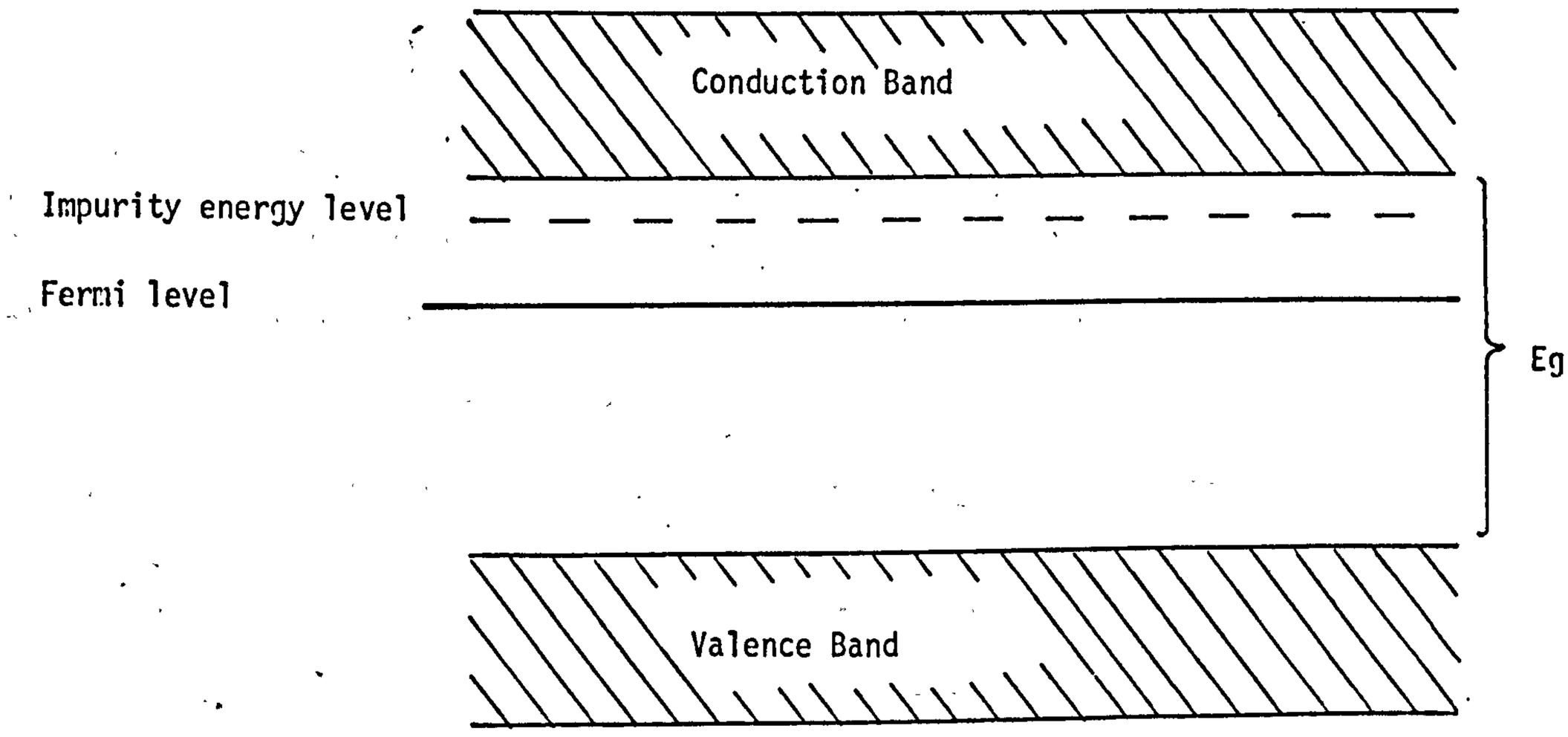

Conduction Band
Impurity energy level
Fermi level
Eg
Valence Band
. Semiconductor without band-gap narrowing
Conduction Band
Fermi level
Impurity Band
ΔEg
Valence Band
Semiconductor with band-gap narrowing

FIGURE 3.12

Without the concepts of heavy doping it is difficult to match observed experimental results to calculation without invoking very short minority carrier lifetimes (high recombination) in regions like the buried N^+. However, experimental results are such that the lifetime in the buried N^+ of Process III devices is large enough (20nS) to allow significant carrier transport and hence collection at the buried N^+ substrate interface. Further aspects of heavy doping are considered in Appendix 7.

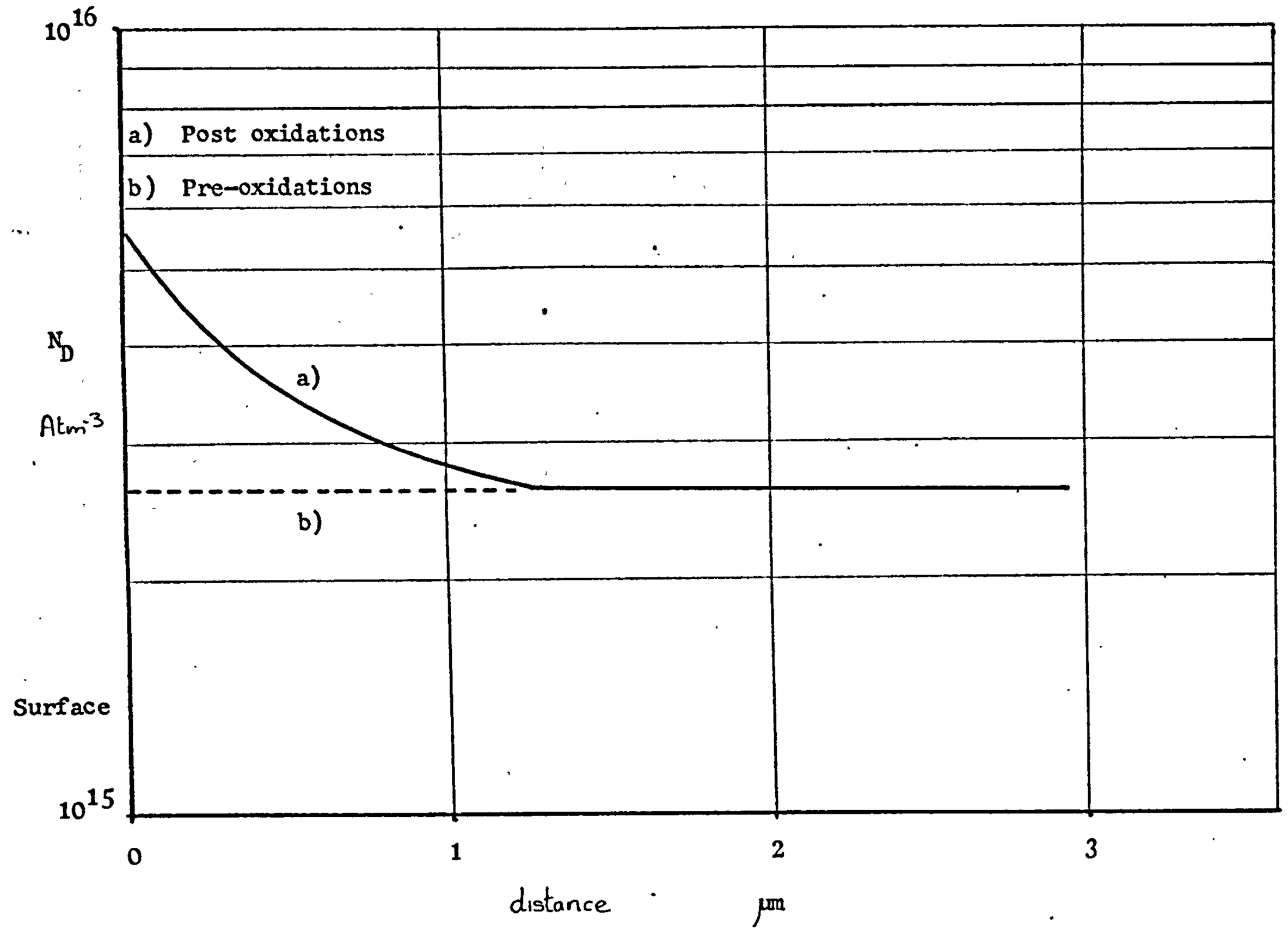
3.3.6. Effective epitaxial doping and surface accummulation of the lateral pnp base.

The magnitude of the lateral re-injection current component of the total I^2L gate base current is heavily dependent on the value of the epitaxy doping in the base region of the lateral pnp transistor. As well as factors determining the minority carrier transport across this lateral pnp base, effects such as surface recombination in the lateral base must be adequately described.

The epitaxy doping of the Process III I^2L gate is effected by many phenomena. In addition to the intentional phosphorus doping added to the growing layer there is buried N^+ up diffusion as a consequence of post epitaxy heat treatments, auto doping of the epitaxial layer by arsenic from the buried N^+ diffusion (34) and the segragation of the epitaxy dopants at the epitaxy surface due to post epitaxial oxidation (35.) Phosphorus is more soluble in silicon than

Figure 3.13

EFFECT OF PROCESS III OXIDATIONS ON EPITAX SURFACE DOPING



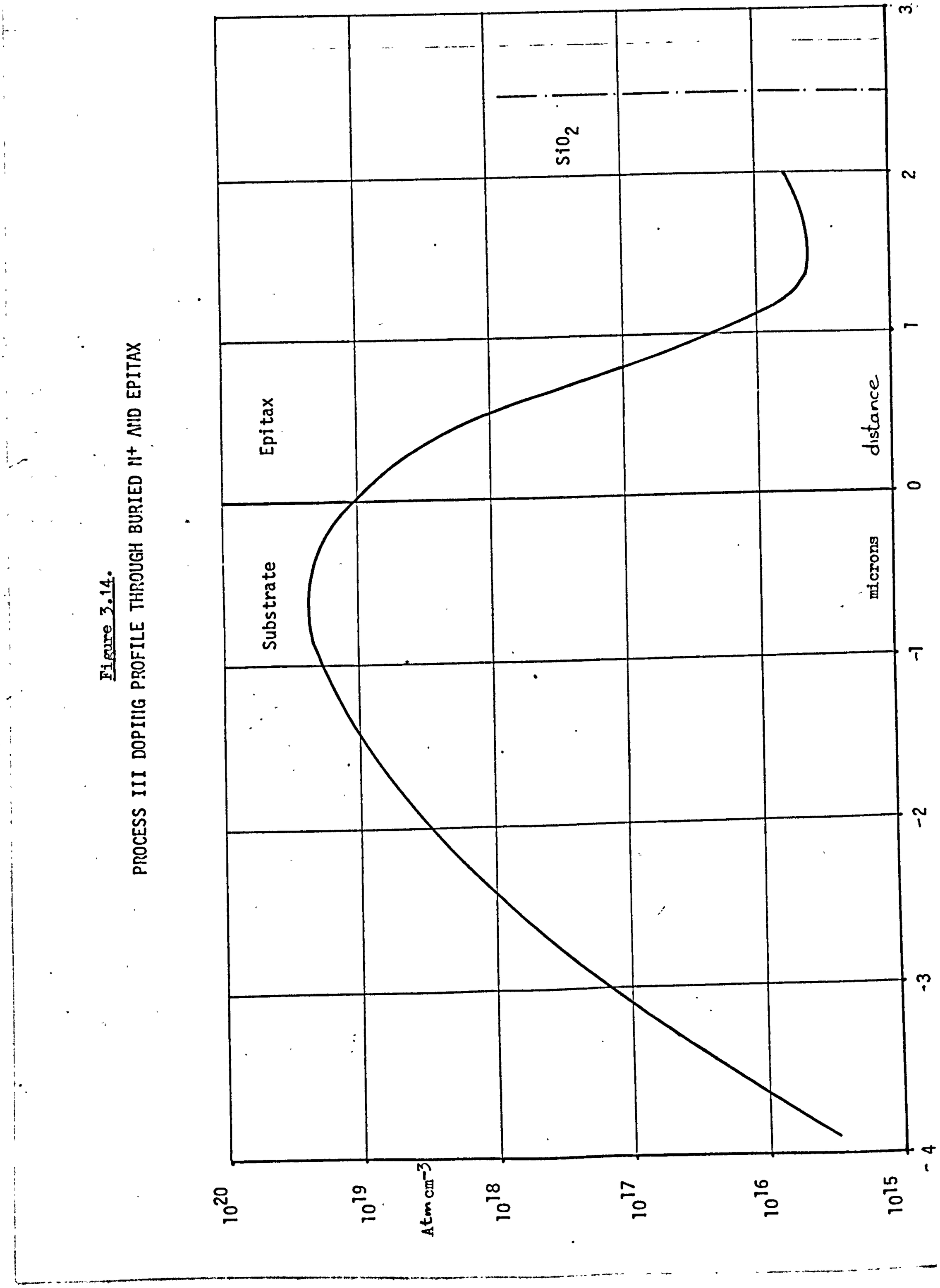


Figure 3.14.

PROCESS III DOPING PROFILE THROUGH BURIED N+ AND EPITAX

silicon dioxide, thus some dopant which was in silicon consumed in oxidation segregates back into the remaining silicon. Figure 3.13 shows the profile of segregated phosphorus as a result of Process III post epitaxy heat treatments. Figure 3.14 shows buried N^+ up diffusion in epitaxy and the buried N^+ substrate diffusion. This data was obtained using a mercury Schottky capacitance voltage probe, bevel and stain, junction depth measurements, and interpolation using the data of Irvin (36).

The above described doping profiles relate to the impurity atoms in the host silicon lattice. However, the charge in the passivating silicon diode also effects the electron (majority carrier) concentration close to the epitaxy surface. The charge associated with the silicon dioxide layer (which is usually positive), - if we assume equilibrium and no net current flow into the oxide surface, - induces an equal and opposite charge in the silicon. The distribution of the charge in the silicon can be calculated as follows:

Since:-

$$J_n = q\mu E\, N(x) + qD_n \frac{dN(x)}{dx} = 0$$

where $N(x)$ is the function describing the induced electron density in the silicon

and $$E = \frac{-KT}{q} \frac{1}{N(x)} \frac{dN(x)}{dx} \qquad 3.12$$

Using Poisson's equation

$$\frac{d^2V}{dx^2} = \frac{\rho(x)}{\epsilon_o \epsilon_r}$$

where $\rho(x)$ is the charge density = $-N(x)q$ in this case

$$\therefore \quad \frac{d^2V}{dx^2} = \frac{-N(x)q}{\epsilon_o \epsilon_r} = \frac{dE}{dx} \qquad 3.13$$

From 3.12 $$\frac{dE}{dx} = \frac{-KT}{q} \frac{d}{dx} \left\{ \frac{1}{N(x)} \frac{dN(x)}{dx} \right\}$$

$$\frac{dE}{dx} = \frac{-KT}{q} \left\{ \frac{1}{N(x)} \frac{d^2N(x)}{dx^2} - \left\{ \frac{1}{N(x)} \right\}^2 \left\{ \frac{dN(x)}{dx} \right\}^2 \right\} \qquad 3.14$$

equating 3.13 and 3.14.

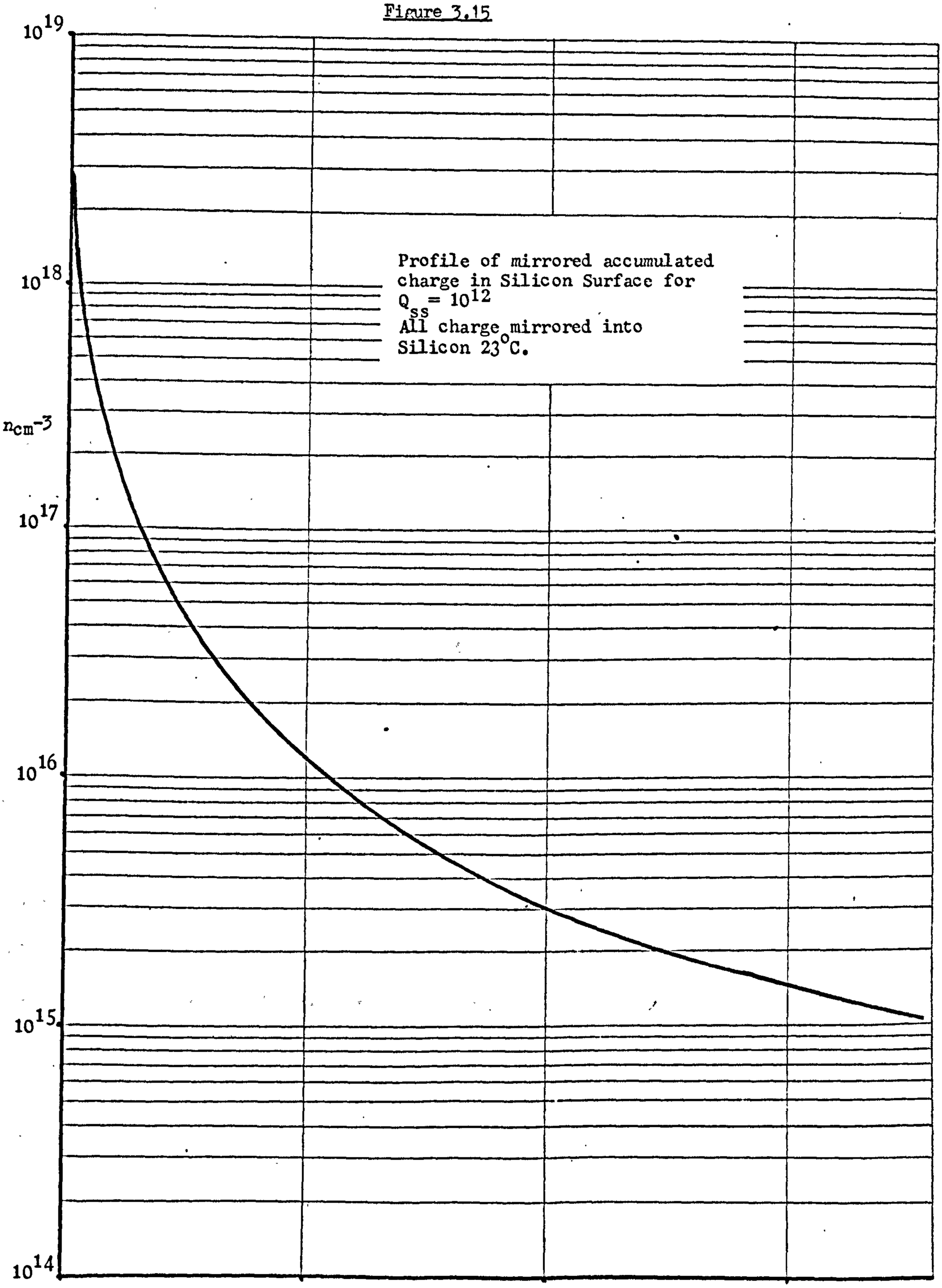
$$\frac{d^2N(x)}{dx^2} - \frac{1}{N(x)} \left(\frac{dN(x)}{dx} \right)^2 - \frac{(N(x)q)^2}{KT \epsilon_o \epsilon_r} = 0 \qquad 3.15$$

if N_{SS} is the oxide charge density, then the solution of 3.15 is

$$N(x) = \frac{2KT \epsilon_o \epsilon_r}{q^2 \left\{ \frac{2KT \epsilon_o \epsilon_r}{q^2 N_{SS}} + x \right\}^2}$$

This function is shown in Figure 3.15 for typical oxide parameters. The effect of this charge accummulation and the dopant segregation is to keep minority carriers away from the silicon surface. Thus surface recombination in the lateral pnp base is unlikely and no experimental evidence exists for supposing that it is a significant component of lateral pnp base current. The other consequence of this non-uniformity of epitaxial doping is that epitaxial doping is higher than the intentional doping and a true average doping is necessary for current calculations. An accurate calculation of the

Figure 3.15


10^{19}
10^{18}
$n_{cm^{-3}}$
10^{17}
10^{16}
10^{15}
10^{14}
Profile of mirrored accumulated charge in Silicon Surface for $Q_{ss} = 10^{12}$
All charge mirrored into Silicon 23°C.
0
0.05
0.1
0.15
µm

current in the lateral base is possible using an extension to the treatment of Moll and Ross (37).

The collected current (I_C) is given by:

$$I_C = \frac{qn_i^2 \; D \; A}{\int_0^{W_B} N \; dx} \quad \exp\,(qV/KT)$$

Where $\int_0^{W_B} N \; dx$ is the integral of the base doping. Sectioning the base into filaments of uniform doping parallel to the silicon surface yields the following for re-injection current formula:-

$$I = qn_i^2 \; A \int_0^{x_j + W_E} \frac{D}{\int_0^{W_B} N d\alpha} dy \; \exp(qV/KT)$$

3.4. COLLECTOR CURRENT OF THE I^2L GATE

The collector current of the I^2L gate is most simply derived by considering extensions to the treatments proposed by Moll and Ross (37), commencing with the hole and electron current equations for the region between emitter diffusion and epitaxy.

$$J_n = q\mu_n \, nE + qDn \frac{dn}{dx}$$

$$J_p = q\mu_p E p - qDp \frac{dp}{dx}$$

As the device is an npn transistor assume:-

$J_n > J_p$ this is valid for the intrinsic base region of the I^2L gate i.e. the region below shallow N^+ diffusion,

if $J_p \rightarrow 0$

$$J_n = qDn \left(\frac{dn}{dx} + \frac{n}{p} \frac{dp}{dx}\right)$$

$$J_n = \frac{qDn}{p} \frac{d(np)}{dx} \quad \text{Assuming Dn constant}$$

$$\int_0^{W_B} pdx = \frac{qDn}{J_n} \int_0^{W_B} \frac{d(np)}{dx} . dx$$

at $x = 0$, $n_o p_o = n_i^2 \exp qV/KT$ at $x = W_B$ $n_o p_o = 0$

$$\int_0^{W_B} pdx = \frac{qDn}{Jn} n_i^2 \exp (qV/KT)$$

and

$$J_n = \frac{qDn . n_i^2 \exp (qV/KT)}{\int_0^{W_B} pdx}$$

In section 3.3.2. it was shown that the effective base region in conditions where there is a large majority carrier current, would be swept out from the base across the low doped epitaxy to the buried N^+ boundary. The hole density in this region must be added to the integral of the base hole concentration.

$$\int_0^{W_B} pdx \simeq \int_0^{W_B} N_A dx + \left\{\frac{n_o \cdot W_B}{2}\right\} + P_o \cdot W_E$$

where n_o is the injected electron level at the base edge and we assume that charge neutrality prevails and excess electrons fall to zero at collector junction ((shallow N^+). P_o is hole concentration at the epitaxy base junction and

we assume negligible recombination in the epitaxy. As the base is formed by diffusion the acceptor and donor concentrations on either side of the base epitaxy depletion region will be approximately equal, i.e.

$$p_o \simeq n_o$$

and $$\int_{W_B} p\,dx \simeq \int_{W_B} N_A\,dx + p_o.(W_E + \frac{W_B}{2})$$

where $p_o = \left\{\frac{N_D^2}{4} + n_i^2 \exp(qV/KT)\right\}^{\frac{1}{2}} - \frac{N_D}{2}$ From equation 3.1.

Figure 3.16 shows plots of the calculated value of I_C v. V_{be} for an I^2L collector.

An experimental observation on Process III (Chapter 6, Appendix 1) is that in the medium injection regime downward gain is controlled by integrated base doping. For a given base bias current is essentilly constant between devices from different slices.

$$\beta_d = \frac{I_C}{I_B}$$

$$\beta_d = \frac{qn_i^2 D \exp qV/KT}{\int N_A\,dx} \cdot \frac{1}{I_{BO} \exp qV/KT}$$

$$= \frac{qn_i^2 D}{\int N_A dx} \cdot \frac{1}{I_{BO}^2}$$

as I_{BO} is constant and contains q and n_i

$$\beta_d = \int \frac{D}{N_A dx} \cdot \frac{1}{\text{constant}}$$

$$\int \frac{D}{N_A}\,dx = \beta_d \cdot \text{constant}$$

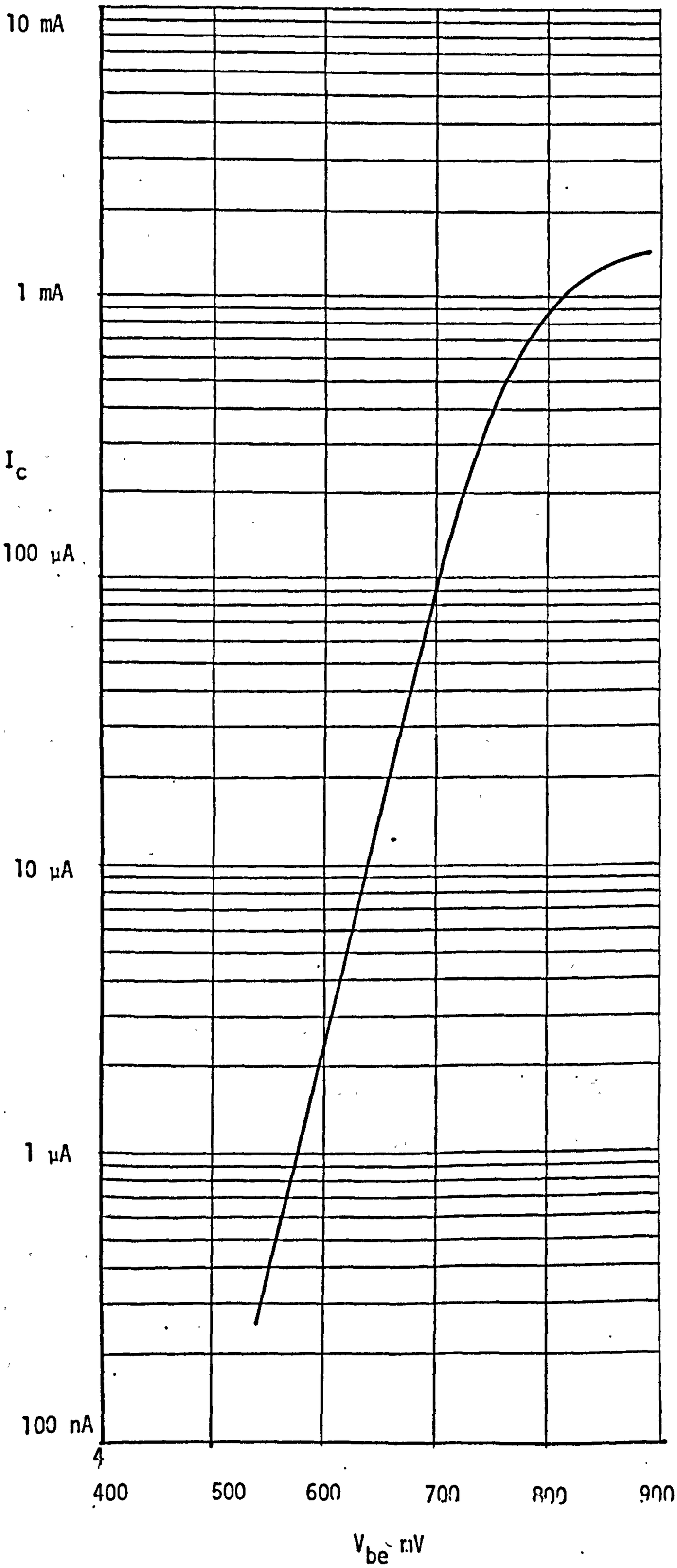


FIGURE 3.16

CALCULATED

PROCESS III

I_c v. V_{be}

The integrated base doping is the same for the downward and upward transistor. If an average value is assigned to D, βd can be used to specify base integrated doping for the upward transistor. βu and βd are related in Process III I^2L by a common base doping. In Process D a similar relationship was found.

3.5. CALCULATED RESULTS

The various phenomena which determine the magnitudes of the injected currents in the I^2L gate structure have been described in the previous part of this chapter. Using these equations the upward gain characteristics of I^2L gates manufactured on three different silicon bipolar processes have been calculated, using a computer programme. The processes are:

Plessey's Process III - a shallow diffused high speed process ($f_T \sim 2$ GHz)

Process D - an 'industry standard' process (base junction depth 2.5μ m, 10μm epitax, 300 MHz f_T).

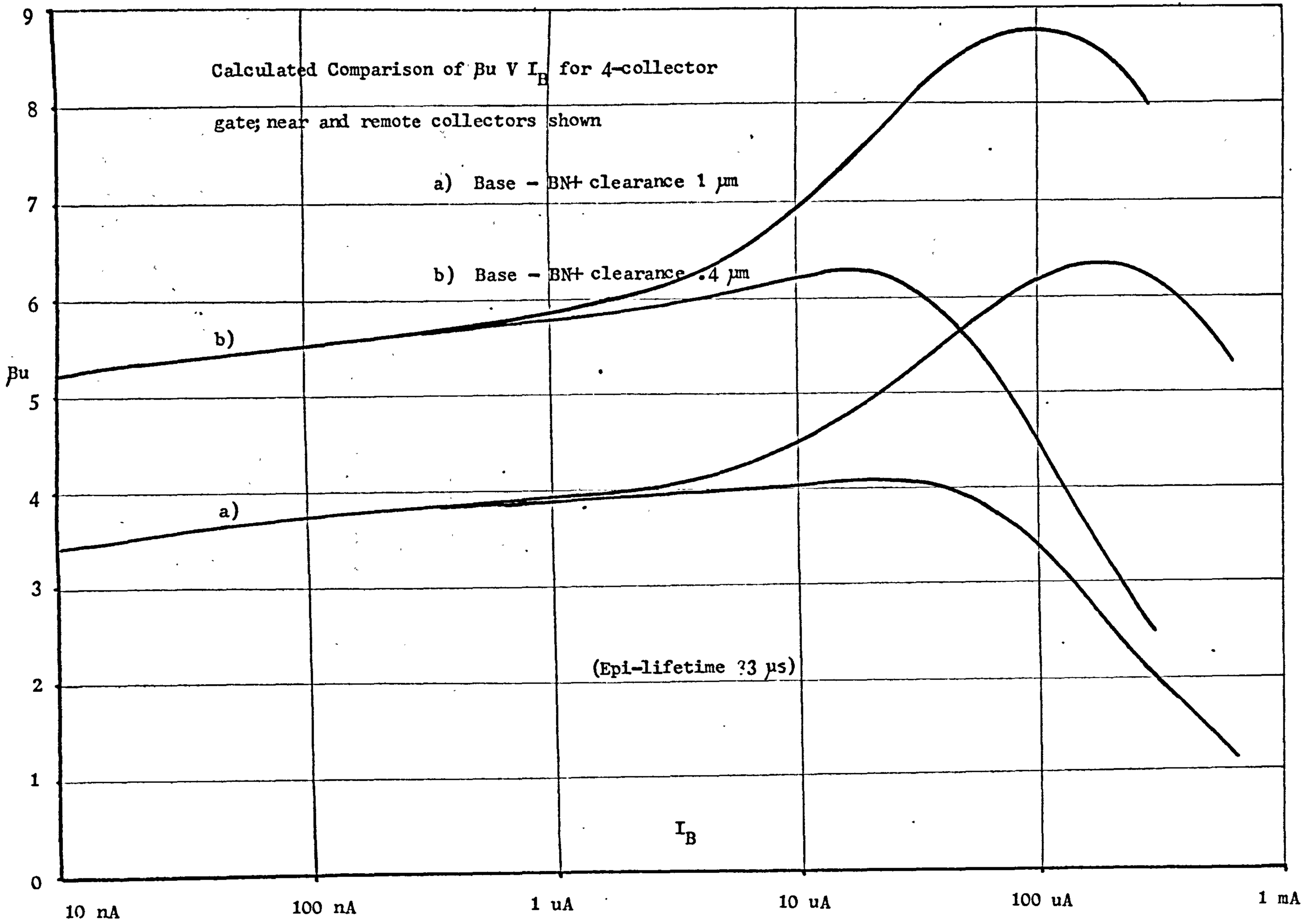
Process H - a high voltage process specifically designed to implement bipolar functions operating from a fifty volt supply.

These processes are discussed in detail in Appendices 1 and 2.

3.5.1. Process III Calculated Results

Figure 3.17 shows the calculated results for βu v I_B of a four collector gate, the characteristics of the collector

Figure 3.17


Calculated Comparison of βu V I_B for 4-collector gate; near and remote collectors shown
a) Base – BN+ clearance 1 μm
b) Base – BN+ clearance .4 μm
(Epi-lifetime ?3 μs)
βu
I_B
9
8
7
6
5
4
3
2
1
0
10 nA
100 nA
1 uA
10 uA
100 uA
1 mA

nearest and most remote from the injector are shown. The effect of varying the epitaxy thickness (base buried N^+ clearance) on the gain is also shown. These results relate to the device for which experimental results are presented in Chapter 5, Figure 5.1.

Using these techniques it is possible to investigate the effect of changing parameters such as surface geometry, doping levels, recombination rates etc.

As the lateral re-injection current is a large component of base current the effect of changing this component on total device performance is of special interest. Figure 3.18 shows the effect of changing the drawn base width of the lateral transistor. This result is substantiated by experiment.

The $\beta_{u\ v}\ I_B$ characteristic of the device appears to be partitioned into two regions, high and low current behaviour.

The low current behaviour is dominated by depletion region recombination. The initial high current behaviour of the collector nearest the injector is controlled by current crowding effects which proportionately increases the base current for that collector. At very high currents β roll's off due to high level injection conditions in the epitaxy. The high current behaviour of the remote collector appears to be dominated by base current starvation due to current crowding, that is resistive debiasing.

The value of βu was shown to be dependent on βd. With the previously developed relationships for base current

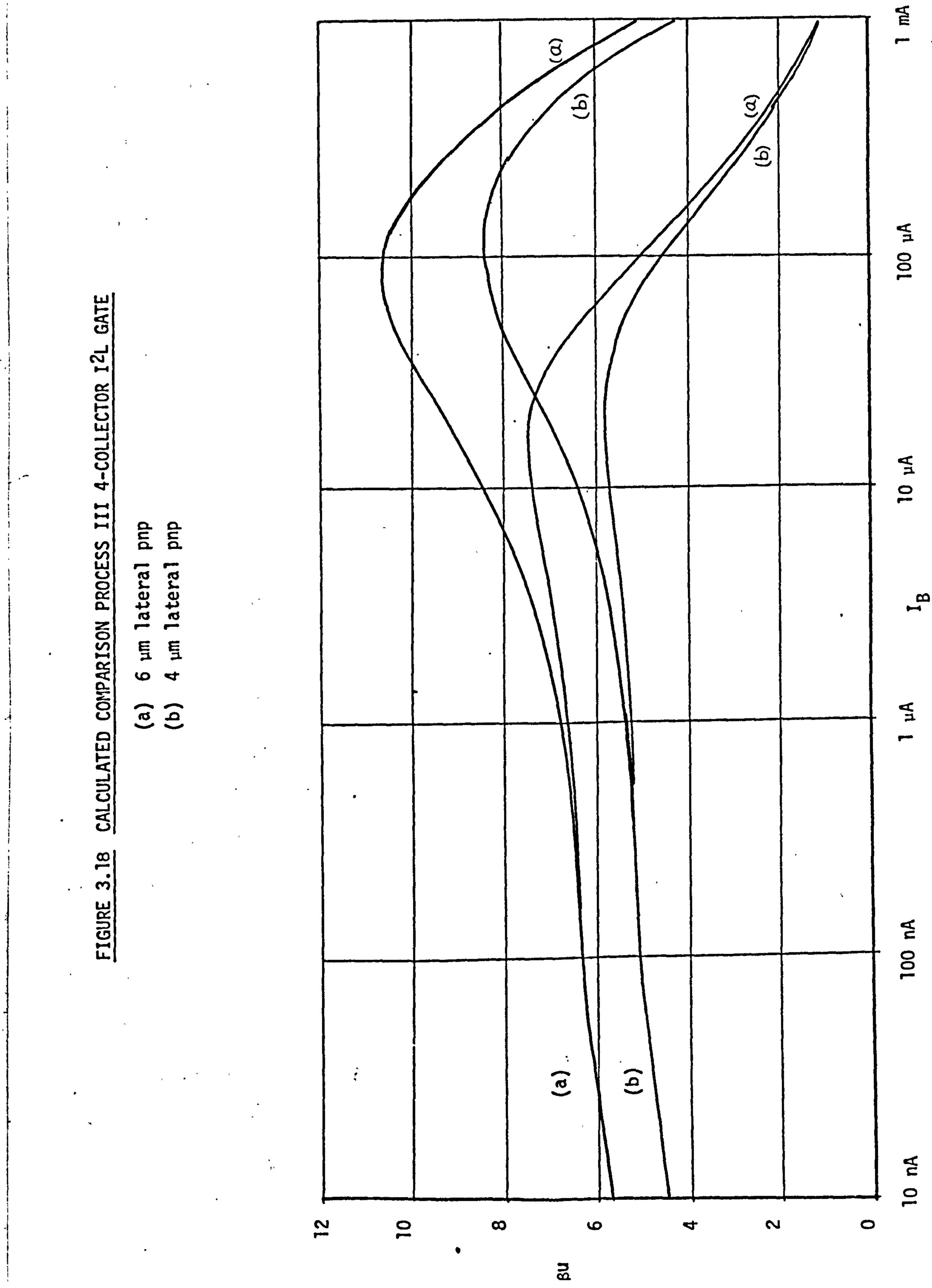


FIGURE 3.18 CALCULATED COMPARISON PROCESS III 4-COLLECTOR I^2L GATE

(a) 6 µm lateral pnp
(b) 4 µm lateral pnp

it is possible to calculate the dependency of βu on W_{epi} (base-buried N^+ clearance) and βd. The hole component of base current in I^2L is dependent on W_{EPI} from two effects: volume recombination in the epitaxy and two dimensional current flow associated with lateral re-injection. Figure 3.19 shows βu at medium currents as a function of W_{EPI} for various values of βd. Figure 3.20 shows a similar relationship but this figure assumes the lateral re-injection to be invariant. This result shows clearly that the dependence of βu on W_{EPI} is dominated by the lateral re-injection component of base current. Volume recombination in the epitaxy is small compared to other components. Electron current lost in oxide covered base regions and hole current in buried N^+ are assumed invariant in these calculations.

In Chapter 6 it is shown that the collector base breakdown voltage BV_{CBO} is related to W_{EPI}. This relationship is shown on Figure 3.19. If the downward gain of the npn transistor and BV_{CBO} are known it it possible to estimate the gain of the upward transistor. These relationships are of significant importance in establishing the compromises for I^2L on a particular process. For example is TTL compatibility compatible with I^2L operation?

3.5.2. Process D Calculated Results

The calculated results for βu v I_B of a four collector Process D I^2L gate are shown in Figure 3.21 for collectors

FIGURE 3.19

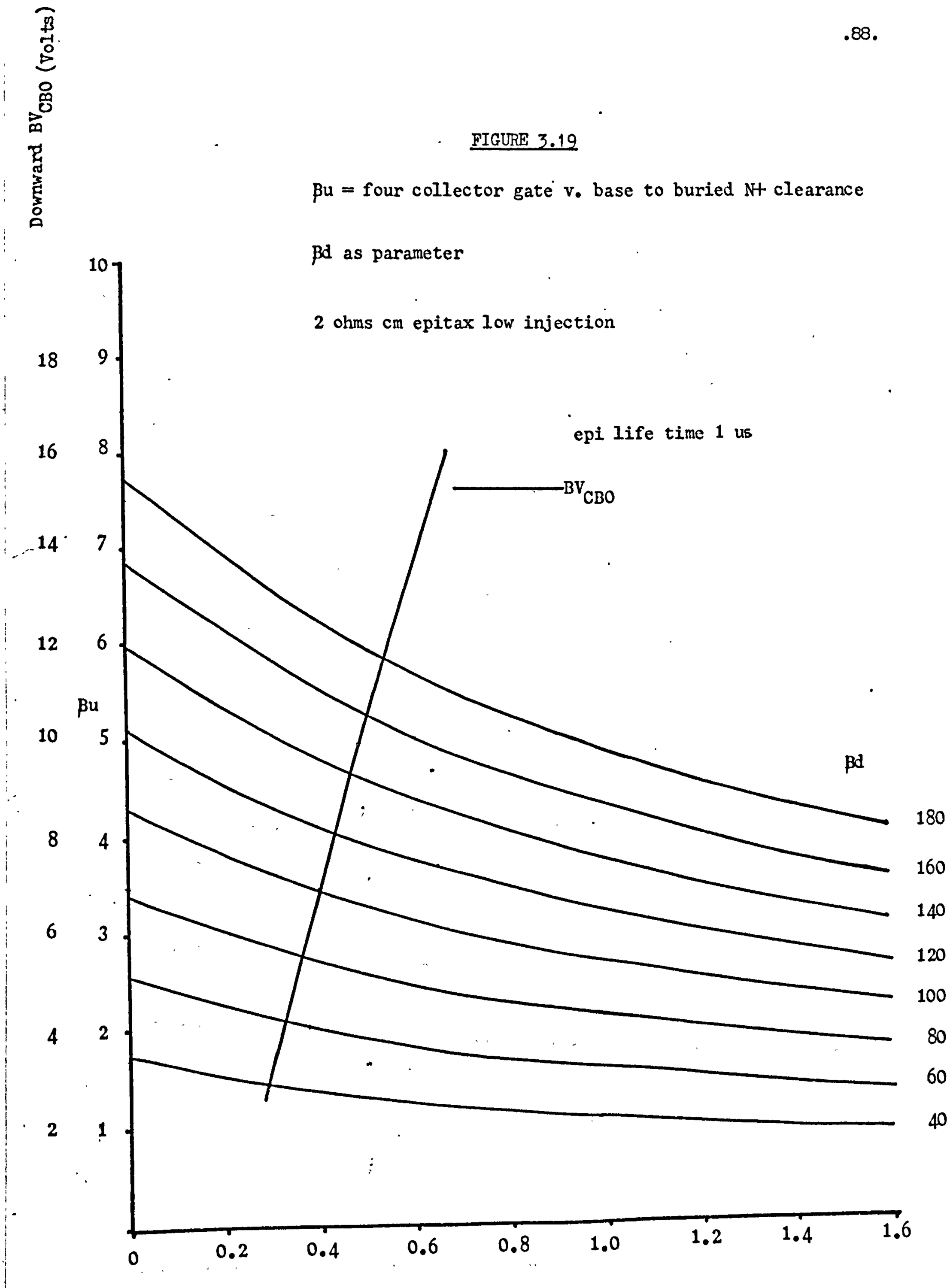

βu = four collector gate v. base to buried N+ clearance
βd as parameter
2 ohms cm epitax low injection
epi life time 1 us
Downward BV_{CBO} (Volts)
BV_{CBO}
βu
βd
180
160
140
120
100
80
60
40
10
9
8
7
6
5
4
3
2
1
18
16
14
12
10
8
6
4
2
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
Base – Buried N+ Clearance μm

FIGURE 3.20

βu Four-Collector Gate v. Base Buried N+ Clearance

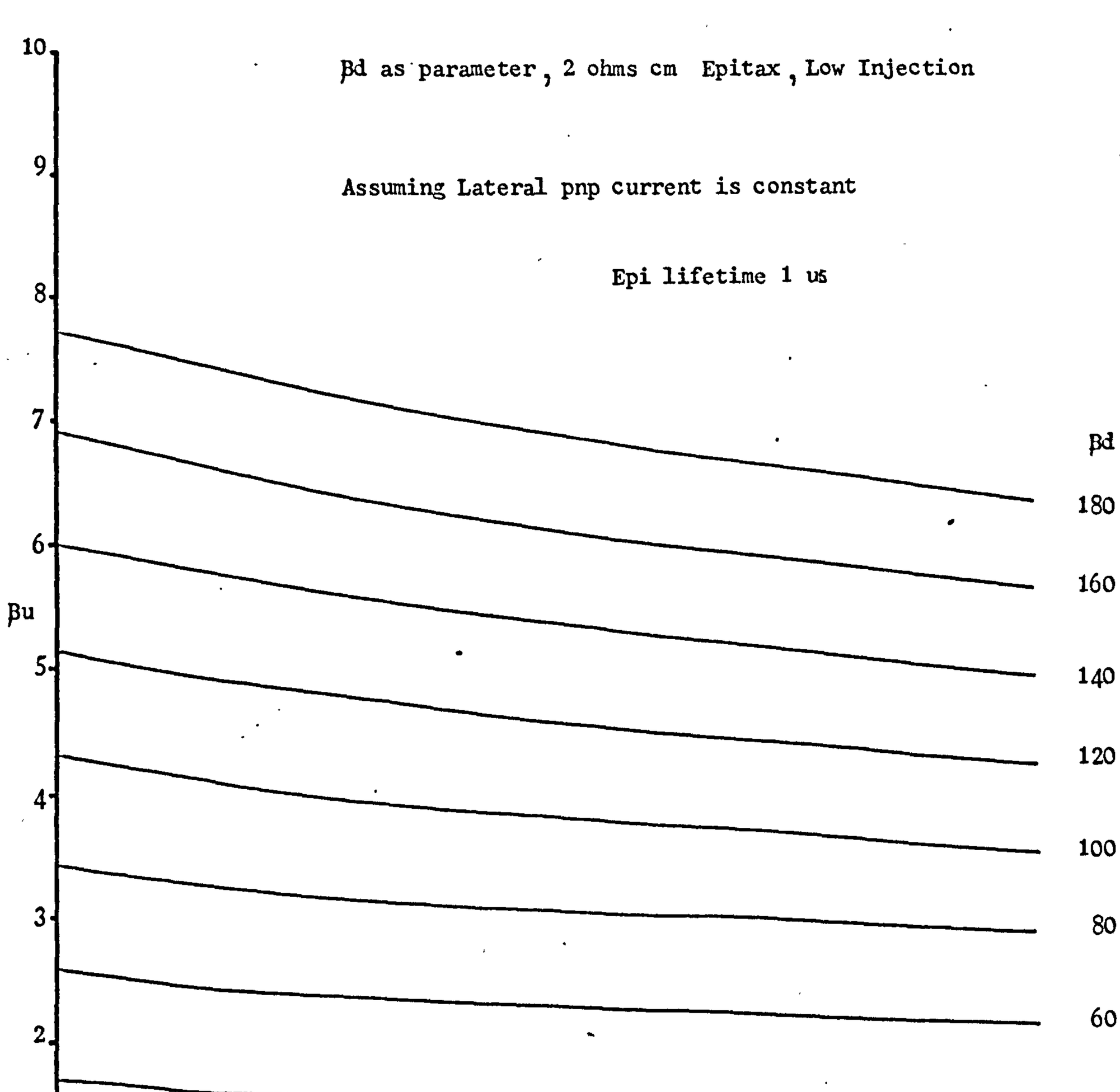
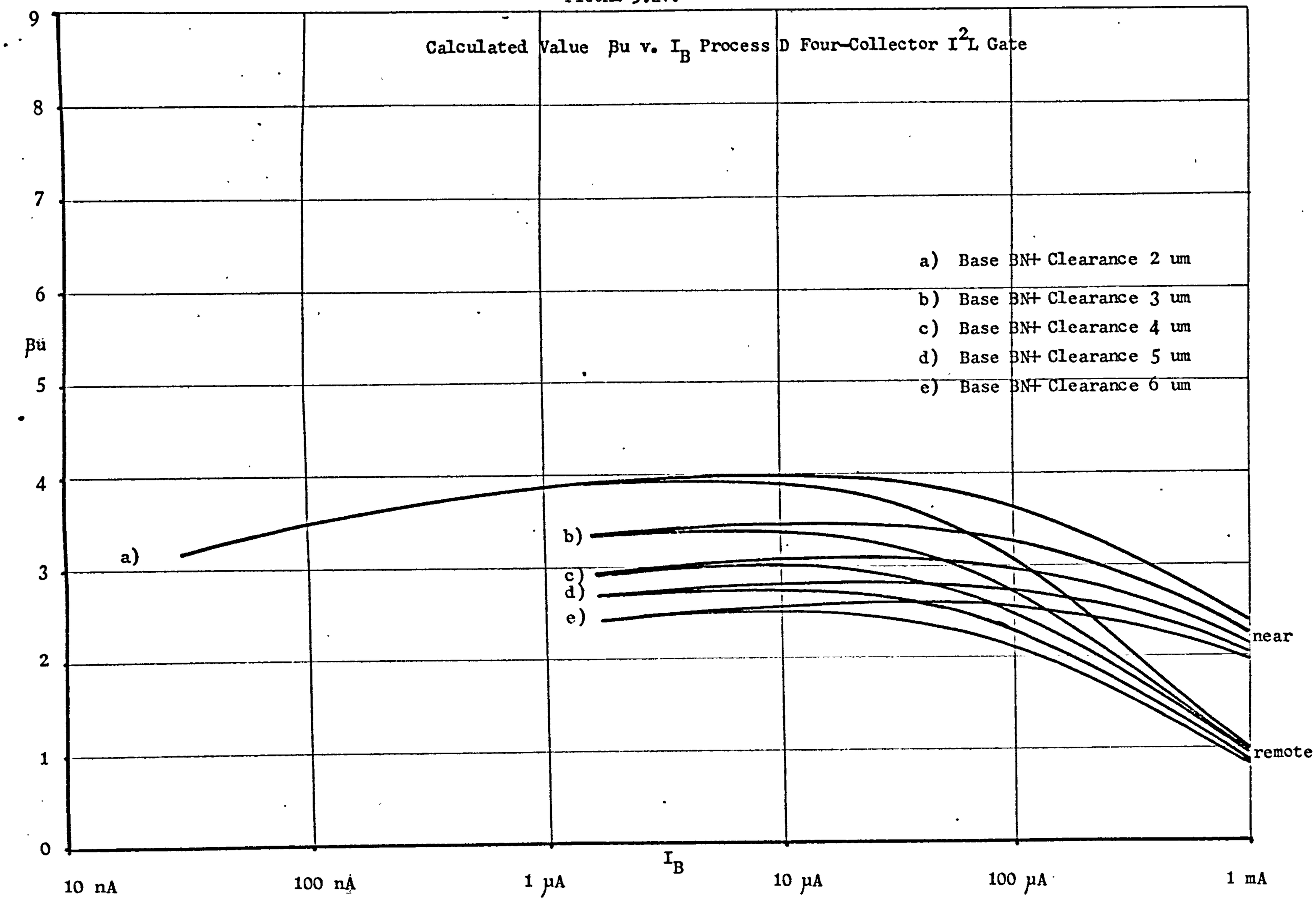


FIGURE 3.21.


Calculated Value βu v. I_B Process D Four-Collector I^2L Gate
a) Base BN+ Clearance 2 um
b) Base BN+ Clearance 3 um
c) Base BN+ Clearance 4 um
d) Base BN+ Clearance 5 um
e) Base BN+ Clearance 6 um
βü
9
8
7
6
5
4
3
2
1
0
near
remote
10 nA
100 nA
1 µA
10 µA
100 µA
1 mA
I_B

Calculated Value βu v. I_B Four-Collector I^2L Gate Process D

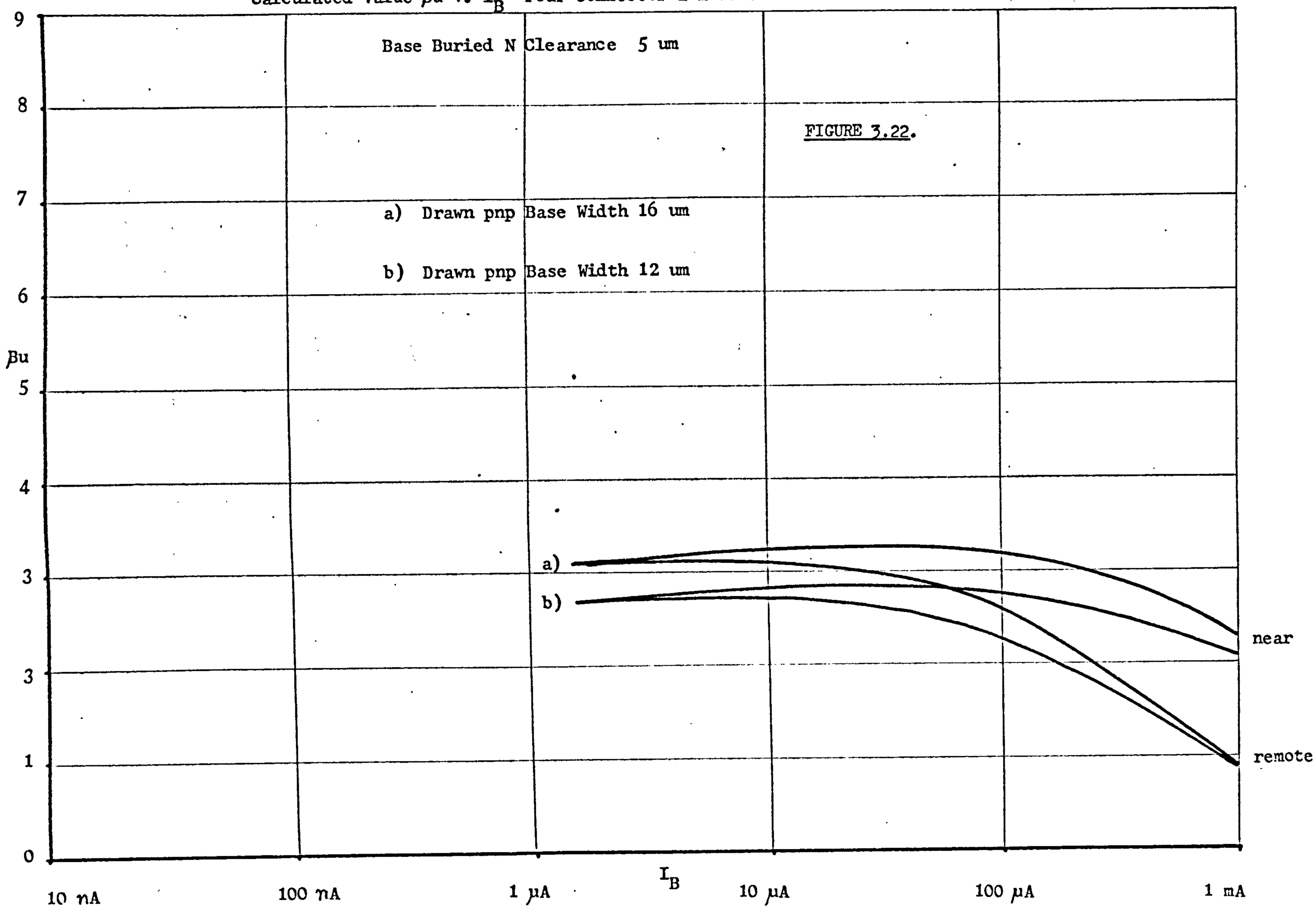


FIGURE 3.22.

near and most remote from the injector shown. The effect of varying the epitaxy thickness on the β u characteristic is also shown. Figure 3.22 shows the effect of varying the lateral pnp base width. The characteristic shown in Figure 3.21 corresponds to the device whose experimental characteristics are shown in Chapter 6, Figure 5-12.

The major parametric difference introduced into the Process D calculation was the value of surface depletion layer recombination velocity. The Process D device is manufactured on ⟨111⟩ orientated silicon as opposed to Process III ⟨100⟩ . As no experimental values of surface recombination velocity were available an arbitrary value of three-times the Process III value was used (see 37, p.342).

The base sheet resistivity of Process D is approximately one third that of Process III; this with the geometry of the Process D device, results in significantly less resistive debiasing. This is shown in a comparison of Process D Process III high current roll-offs for near and remote collectors.

3.5.3. High Voltage Process Calculated Results

The mask set designed for use with the Process D I^2L was used to investigate high voltage process I^2L. In order to calculate the high voltage I^2L characteristics a device geometry identical to that of the Process D device was used. The calculated results were obtained before any devices had

FIGURE 3.23

HIGH VOLTAGE PROCESS I^2L

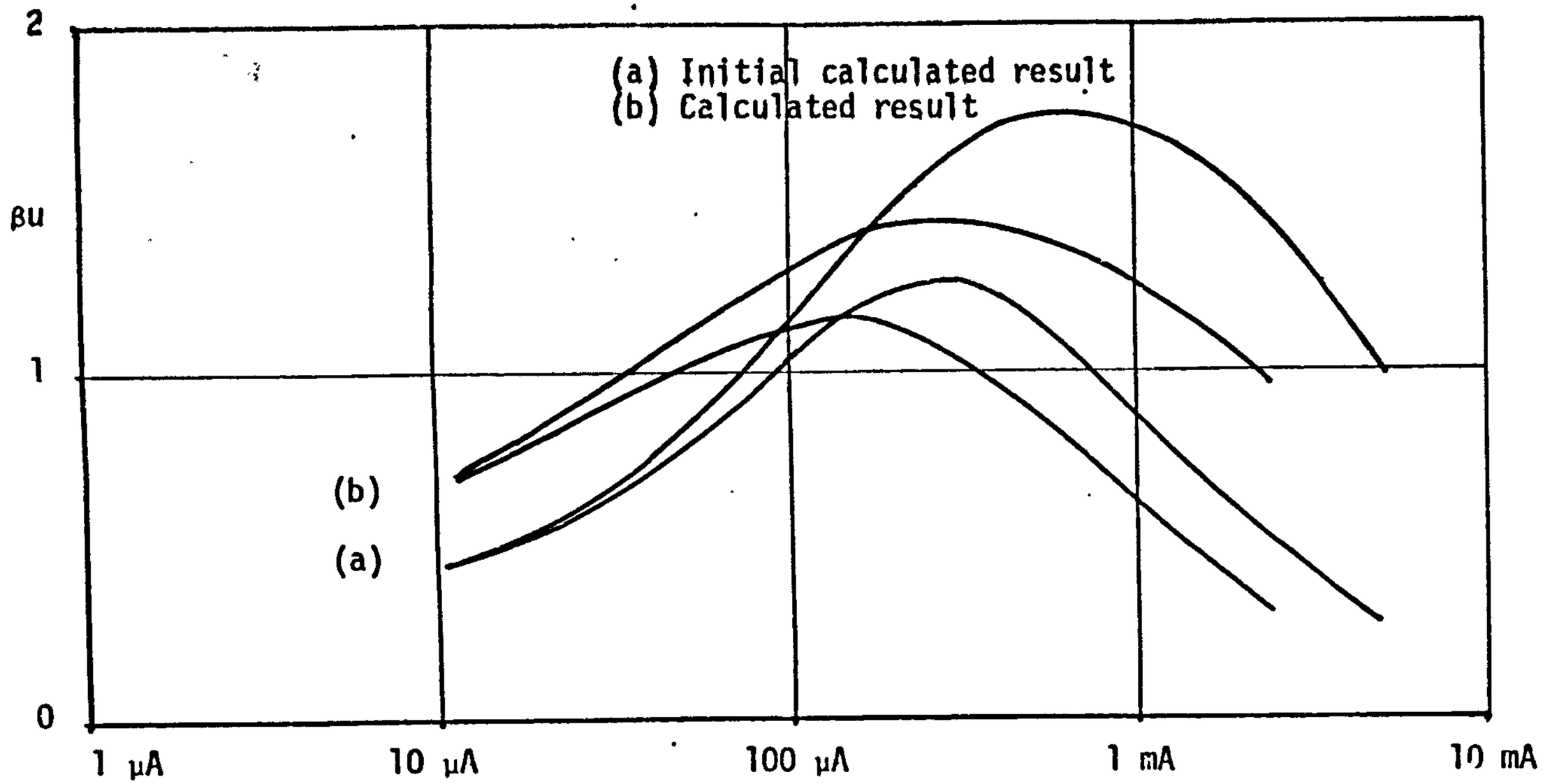
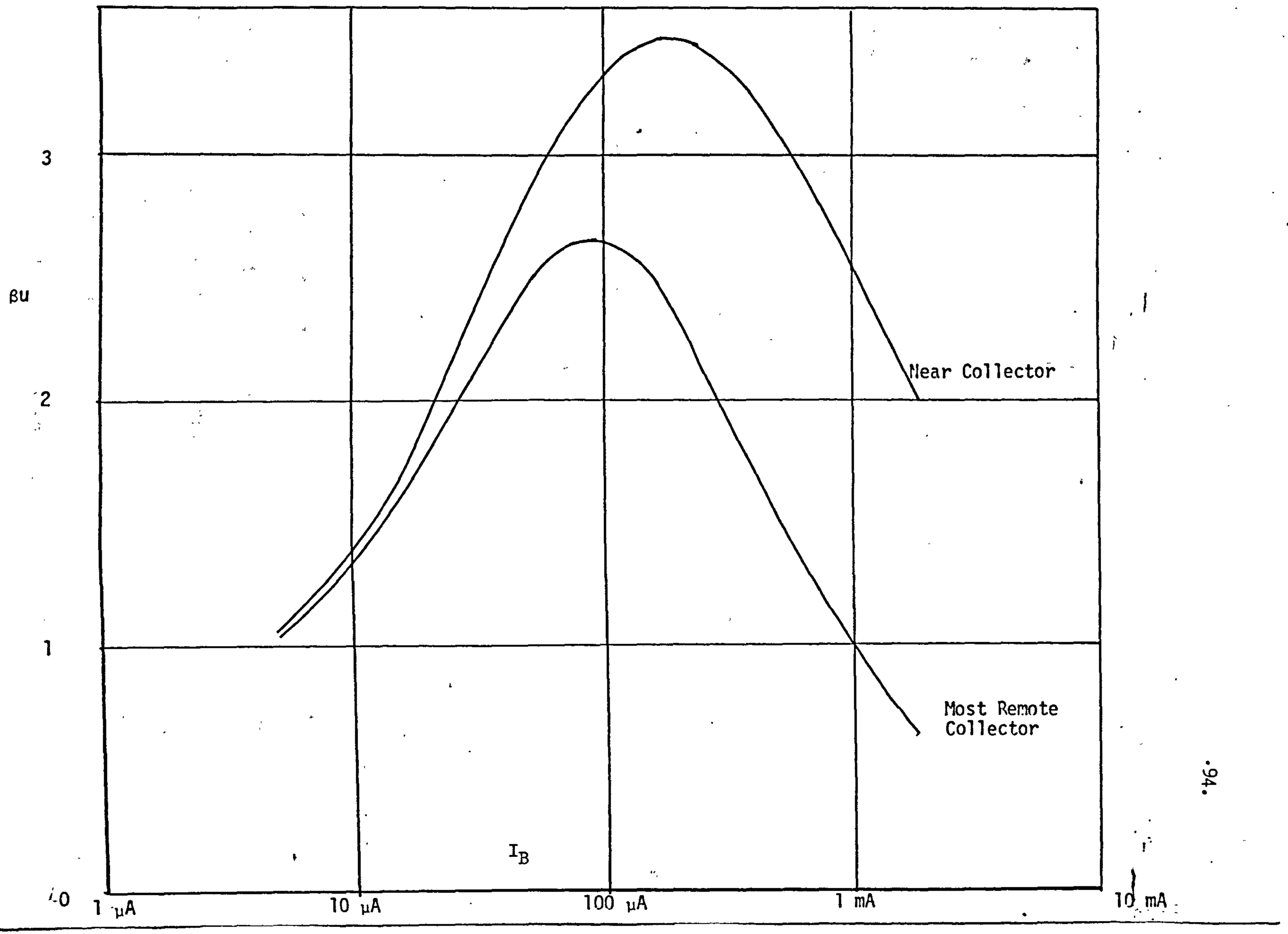


FIGURE 3.24

PROPOSED HIGH VOLTAGE GATE CHARACTERISTIC



been fabricated. Figure 3.23 shows two calculated results. The results of initial calculations before the fabrication of actual devices, clearly indicate that I^2L on this process will not function, as βu is not larger than two. When more accurate data became available as a consequence of experimental device investigations, the characteristic was re-calculated, and this resulted in a closer fit with experiment (see figure 5.14).

The calculations could be made to agree closer with experiment by suitable manipulation of such parameters as lifetimes and effective dopings etc. However this is not the point of the excercise which is to demonstrate that the mechanisms controlling device behaviour are understood.

The results for the high voltage I^2L gate show that a structure similar to that used for Process D is unsuitable. A design excercise using the previously described relationships and the computer program was undertaken. The results from this are shown in Figure 3.24. A device with suitable characteristics for I^2L operation. This device is described in Appendix 2.

At this time the proposed structure has not been manufactured.

3.6 Discussion.

The mechanisms controlling the D.C. characteristics of the I^2L gate have been described. New expressions have been developed to describe these major effects. Although these expressions are subject to a number of simplifying approximations in their derivations, the calculated behaviour of the device (see Ch 5) is in close agreement with experimental observations. This is verified for results from three different processes.

The gain of the I^2L device in the upward mode is shown to

be dependent on recombination in the epitaxy, surface recombination in the base, the lateral re-injection current (which in turn is dependent on epitaxy thickness and lateral pnp base width). The gain is also shown to be dependent on the integrated doping in the intrinsic base region.

The high current operation of the devices is shown to be heavily dependent on resistive debiasing/current crowding effects.

The debiasing causes an initial increase in gain for the collector nearest the injector and a loss gain for the remote collector as the device moves into the high current regime. These effects are felt on a proportional basis for the 'second and third' collector.

CHAPTER 4

SWITCHING THEORY OF I^2L GATES

4.1. INTRODUCTION

The D.C. behaviour of the I^2L gate has been described in the preceding chapter. The object of this chapter is to describe the switching theory of the I^2L gate. The switching characteristics of the I^2L gate are heavily dependent on its D.C. behaviour, debiasing, injected carrier profiles, etc. The results for the D.C. characteristics will be used to assist in the explanation of the switching behaviour.

As an introduction a brief summary of the available published works will be given.

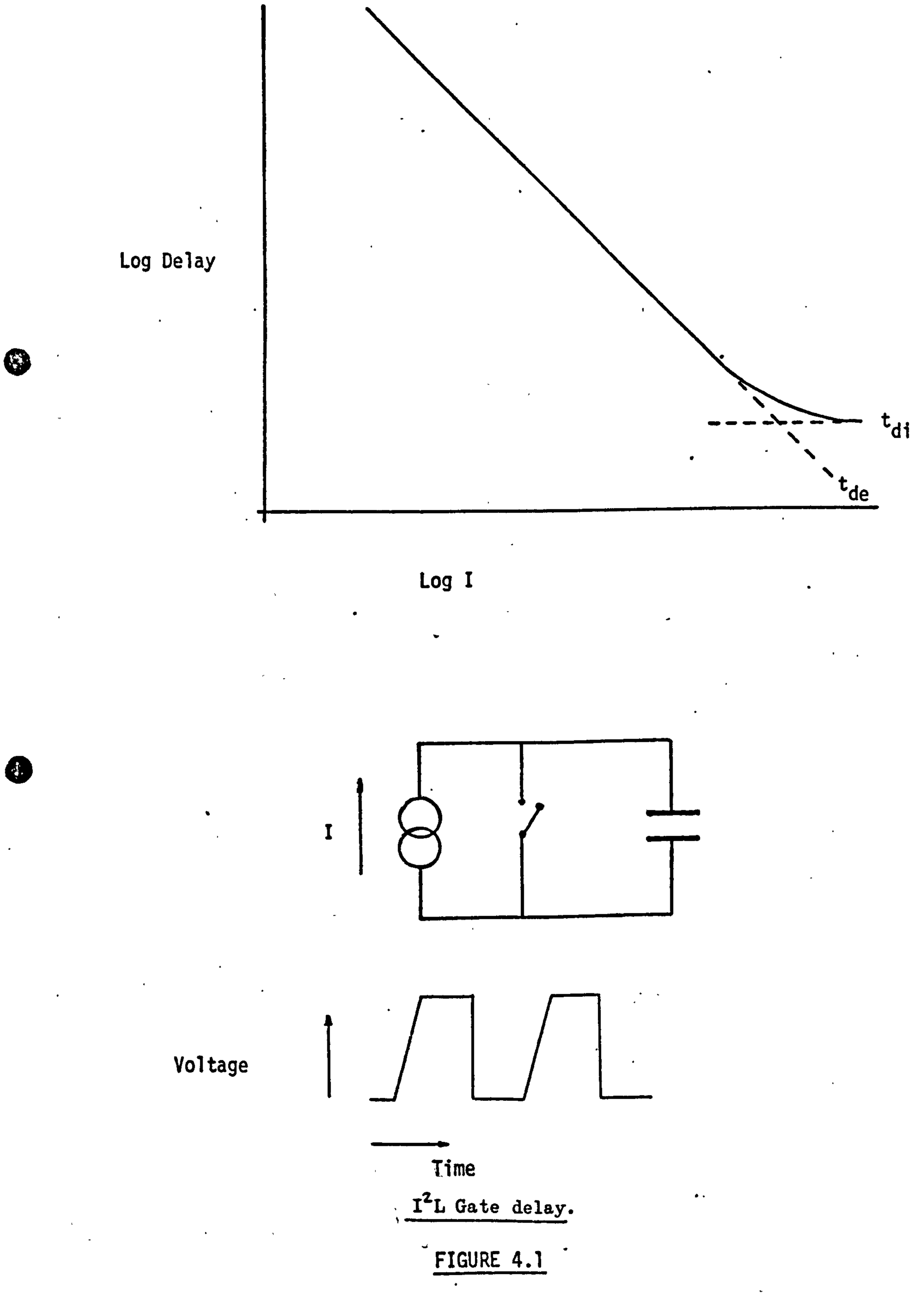
4.2. THEORIES OF WEIDMANN AND BERGER

Weidmann and Berger (12) and Berger (14) use an Ebers Moll terminal model to simulate the switching delay characteristic of an I^2L device. The switching delay is shown to consist of two parts:-

Part 1. The extrinsic delay $\bar{t}_{de}$ due to depletion, stray and load capacitances.

Part 2. The intrinsic $\bar{t}_{di}$ delay due to minority carrier storage in the device.

The extrinsic delay is inversely proportional to the charging current available, and thus approximately inversely proportional to the supplied D.C. power and injector current. The intrinsic delay does not depend on the available charging current, and is constant with supplied power.



I^2L Gate delay.

FIGURE 4.1

The extrinsic delay is approximated by:

$$\bar{t}_{de} \simeq \frac{1}{2}\frac{\sum C_{v\ eff}}{I_o}\ \Delta V$$

where $\sum C_{v\ eff}$ is the total effective node capacitance and ΔV is logic swing. The components of $\sum C_{v\ eff}$ are estimated by calculating the total charge variation on a node during a logic swing.

The intrinsic delay is shown to be dependent on the magnitudes of upward and downward gain and emitter time constant (ratio of charge stored in the device to emitter current).

The nature of the relationship between switching delay and charging current is that shown in Figure 4.1. with the inset representing the simple equivalent circuit in the extrinsic delay regime.

Berger and Weidmann's calculations predict that $\bar{t}_{di}$ increases with increasing βu. However, in their discussion they point out that this is not necessarily so and, in fact, Berger (14) presents experimental evidence which shows that $\bar{t}_{di}$ decreases with increasing βu. βu was increased by extending shallow n^+ drive-in time. However Berger says that with this procedure $\bar{t}_{di}$ could be further decreased by decreasing βu. This was achieved by increasing the lateral re-injection current of the pnp injector transistor.

4.3. THEORIES OF KLAASEN

Klaasen (15) in a paper on the device physics of I^2L

gives a treatment of the switching of the I^2L gate which is based on the structure of the device. The switching delay is given as the sum of the charging delay associated with depletion and stray capacitance plus a component due to minority carrier storage. The delay associated with the depletion capacitance is derived in a similar way to that of Weidmann and Berger.

However the delay associated with minority carrier storage is treated using charge control theory. Klassen develops an expression for peak f_T of the I^2L gate and relates intrinsic delay to this f_T.

Using charge control theory (39) angular cut off frequency W_T can be defined as

$$\omega_T = \frac{I_c}{Q_{TOTAL}}$$

where I_c is the collector current and Q_{TOTAL} is the total charge stored in the transistor.

Using the treatment of Moll and Ross (37)

$$I_c = \frac{q\, n_i^2\, D_n\, (\exp(qV/KT))\, A_c}{\int N_A\, d_x} \qquad 4.1.$$

where A_c is the collector used.

Klaasen says that the major portion of the stored minority carrier charge, is that due to hole transport across the epitaxy. In Chapter 3 it was shown that carrier level at the buried N^+ epitaxy interface is nearly the same as that at the depletion edge, as a consequence of high carrier lifetime in the epitaxy. This means that $\frac{dP}{dx} \simeq 0$ at the

junction. The total minority carrier stored charge is then

$$Q_T \simeq q \frac{n_i^2 \left(\exp qV/KT\right) . A_B . W_{EPI}}{N_{D_{EPI}}} \qquad 4.2.$$

Where A_B is the base land area, W_{EPI} is base buried N^+ clearance.

Using equations 4.1. and 4.2. in the expression for W_T we have

$$W_T = \frac{Ac}{A_B} \quad \frac{Dn \quad N_{D_{EPI}}}{W_{EPI} \int N_A \, dx} \qquad 4.3.$$

Although this expression gives an intuitive insight into the factors limiting maximum cut-off frequency, it is inadequate in detail. The equations for collector current derived in Chapter 3 section 3.4 was:-

$$I_c = \frac{q \, n_i^2 \, Dn \, \left(\exp (qV/KT)\right) Ac}{\int N_A \, dx + P_o \left(W_B/_2 + W_{EPI}\right)} \qquad 4.3(b)$$

and the charge stored is

$$Q_{TOTAL} \simeq p_o \cdot A_B \cdot W_{EPI} \quad \begin{array}{l} q + \text{Depletion} \\ \text{capacitance components} \end{array} \qquad 4.3(c)$$

$$p_o = \left(N_{D_{EPI}}{}^2/_4 + n_i^2 \exp (qV/KT)\right)^{\frac{1}{2}} - N_{D_{EPI}}/_2$$

($A_B \cdot W_{EPI}$ = effective volume to include lateral pnp storage)

Using the above relationships an improvement to Klaasen's predictions is achieved which enables an accurate calculation of cut-off frequency.

Having developed his expression for cut-off frequency Klaasen then produced the following transcendental equation for intrinsic delay

$$t_{di} = \gamma_{eff}^{1} \ln \frac{2\, t_{di} + \gamma_{eff}^{1}}{\gamma_{eff}^{1} - (2\, \gamma_{1}\, f_T)^{-1}}$$

Where γ_{eff}^{1} is the effective hole lifetime in the epilayer.

Under condition that $t_{di} < 2\, \gamma_{eff}^{1}$

$$t_{di} \simeq \beta_{u}^{1/2} / 4\, \pi f_T$$

In practical structures β_u and f_T are interrelated in such a way as to make the ratio $\beta_u^{1/2}/f_T$ vary inversely with β_u, i.e. t_{di} decreases as β_u increases.

4.4. RESULTS OF OTHER WORKERS AND IMPLICATIONS OF WEIDMANN, BERGER AND KLAASEN ANALYSIS

The publications of Weidmann and Berger and F.M.Klaasen are very comprehensive and cover the major parts of I^2L theory. Most of the remaining publications on I^2L detail experimental results with not much reference to theory.

A paper by Shinozaki et al of Toshiba (40) shows that minimum gate delay t_{di} is proportional to $1/\beta_u^{1/2}$,

$$t_{di} \propto \frac{1}{\beta_u^{\frac{1}{2}}}$$

for large β_u. This result offers an interesting comparison with that of Klaasen. f_T is nearly linearly related to β_u, if both are changed by modifying the integrated base doping. Thus Klaasen's result could be interpreted as

$$t_{di} \propto 1/\beta_u^{1/2}.$$

The intrinsic delay analysis of Weidmann and Berger predicts that t_{di}/τ_e is approximately proportional to $\beta_u^{1/2}$ (interpreting from data). However, τ_e (emitter time constant) is

proportional to $1/\beta_u$. The implications of these predictions for the real I^2L device is extremely subtle.

In the I^2L gate, upward gain β_u can be changed by either:

i) altering collector current by changing integrated base doping, keeping base current constant,

or ii) by changing base current keeping collector current constant.

Similarly cut-off frequency or intrinsic switching speed can be modified by either:

i) changing the amount of stored charge in the gate (which is associated with base current)

or ii) modifying the current available, to control the stored charge, i.e. collector current.

Obviously β_u and intrinsic switching speed are interrelated. Berger and Weidmann suggest that switching speed could be improved by decreasing the lateral base width of the injector transistor. This reduces β_u which according to their analysis will decrease switching speed. However, the charge stored in the saturated lateral transistor is a significant part of the total charge storage, and decreasing the lateral base width by an amount significant enough to modify β_u results in appreciable change in stored charge and thus switching speed.

4.5. GENERAL SWITCHING THEORY

4.5.1. Switching in Constant Power-Delay Product region (Extrinsic delay)

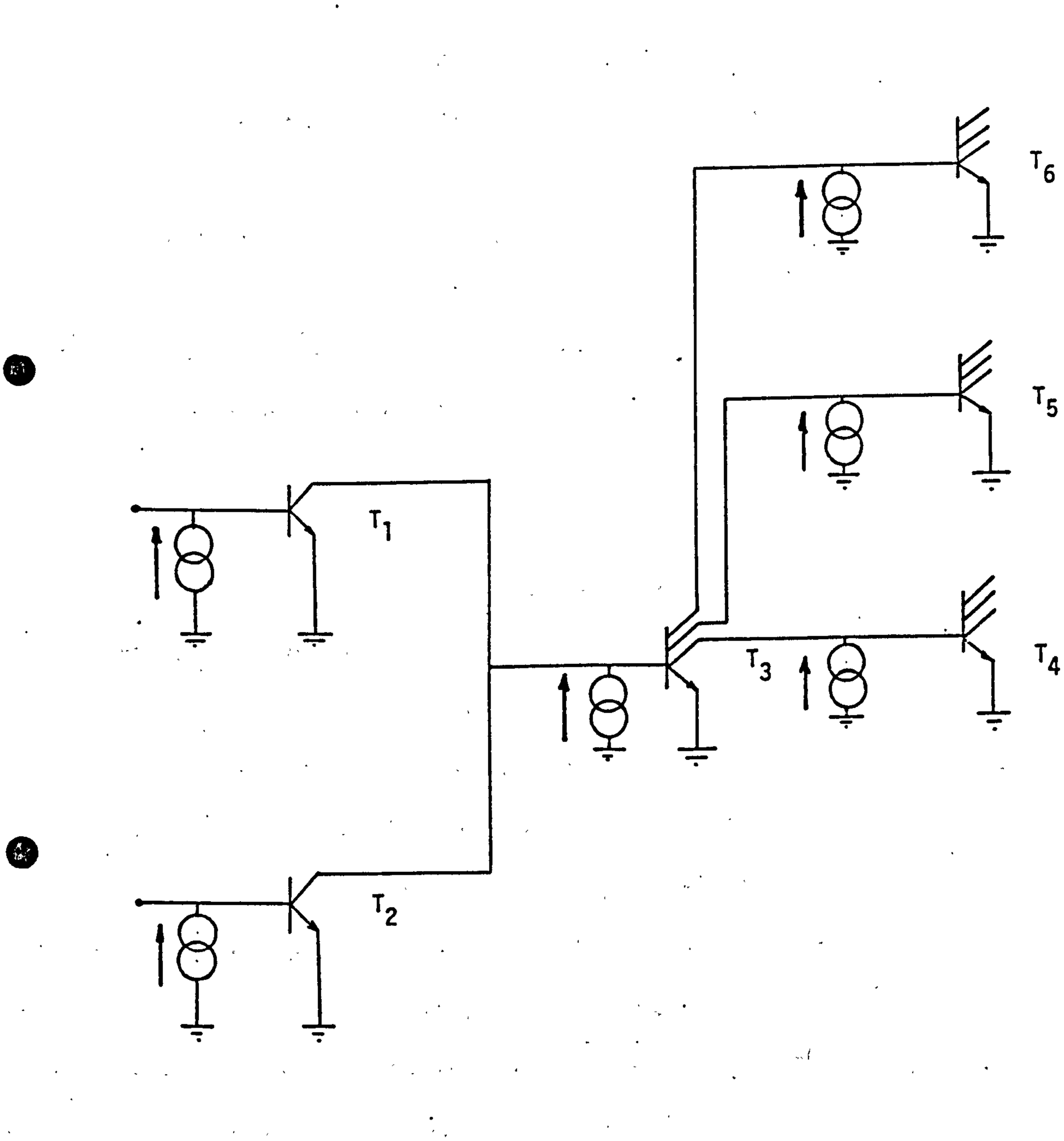


FIGURE 4.2

Circuit used to calculate gate delay in the constant power-delay product regime.

The switching delay of an I^2L gate in its low power operating condition is dominated by the junction depletion region capacitances associated with the base epitaxy junction and the base collector (i.e. emitter diffusion of downward transistor) junctions of the npn device, (this region of operation was previously defined as the extrinsic region).

The capacitance which has to be charged at a gate input is made up of the following components:

1) the emitter base capacitance of the gate.
2) the fan-out capacitance of the gate, i.e. the total capacitance of the collectors on that gate, plus the input capacitance of the following gates.
3) the fan-in capacitance of the gate, i.e. the total number of collectors pulling the input of the gate.

In order to facilitate understanding of the extrinsic switching delay t_{de}, Figure 4.2 shows a hypothetical logic circuit and t_{de} is defined as half the time required for the transition of T_3 to the on state and T_4, T_5 and T_6 collectors to the edge of conduction. The sequence being initiated by the instantaneous switch on of T_3.

The analysis is as follows: The delay period is split into two components, t_1 the time required to bring T_3 from the off condition to the edge of conduction, and t_2 the time from T_3 collectors conducting until T_4, T_5, T_6 collectors are brought to the edge of conduction (i.e.nearly off)

Therefore $$t_{de} = \frac{t_1 + t_2}{2}$$

It is assumed as an initial condition that T_1 is off and T_2 is suddenly switched off, then the base current of T_3 has to charge the emitter base capacitance (C_{eb}) and the collector base capacitances ($3\ C_{cb}$) through V_{be} to bring T_3 to the edge of conduction. Furthermore C_{cb} of T_1 and T_2 must also be charged through this potential. T_3 collectors are at a V_{be} at $t = 0$, and the base is at V_{ce} sat ($\simeq$ 0v) and at the edge of conduction, collectors and base are at a V_{be}, that is $V_{cb} = 0$. Collectors of T_1 and T_2 are at V_{ce} sat. at $t = 0$ and at a V_{be} when T_3 collectors are at the edge of conduction.

The base current i_b in T_3 is given by the following equation:

$$Q = i_b\ t_1 = (n\ C_{cb} + m\ C_{cb} + C_{eb})\ V_{be}$$

$$t_1 = ((m + n)\ C_{cb} + C_{eb})\ \frac{V_{be}}{I_b} \qquad 4.1.$$

using the general case n = numbers of collectors per gate.(fan-out)

m = fan-in of that gate,

and assuming linear charging with voltage.

When T_3 starts to conduct, its collectors are capable of sinking a current $\beta\ i_b$ However the collector must change the charge in its collector base capacitance C_{cb} and the injectors of T_4, T_5 and T_6 are still functioning. Thus in the time interval t_2 the collectors of T_3 are effectively capable of sinking current i_c given by

$$i_c = \beta u \left(i_b - \frac{C_{cb} V_{be}}{t_2}\right) - i_b \qquad 4.2.$$

from the connected gates.

The capacitive term arises in this manner because the current to change the charge must be supplied via the base.

In order to bring T_4, T_5 and T_6 to the edge of conduction the charge which must be removed from their respective capacitances is

$$(C_{eb} + n\,C_{cb})\,V_{be} \qquad 4.3.$$

This charge is removed in time t_2 hence

$$i_c = (C_{eb} + n\,C_{cb})\,\frac{V_{be}}{2\,t_2} \qquad 4.4.$$

Eliminating i_c from equations 4.2. and 4.4.

$$t_2 = (C_{eb} + (n + \beta u)\,C_{cb})\,\frac{V_{be}}{(\beta u - 1) i_b} \qquad 4.5.$$

Now $t_{de} = \frac{1}{2}(t_1 + t_2)$

$$= \frac{1}{2}\left[\frac{(C_{eb} + (n+\beta u)\,C_{cb})\,V_{be}}{(\beta u - 1) i_b} + \frac{V_{be}}{i_b}\left\{\frac{(n+m)\,C_{cb} + C_{eb}}{}\right\}\right]$$

$$t_{de} = \frac{V_{be}\,\beta u}{2 i_b (\beta u - 1)}\left\{C_{eb} + \left(1 + n + m - \frac{m}{\beta u}\right) C_{cb}\right\} \qquad 4.6.$$

Equation 4.6. can be used to describe gate delay as a function of device parameters.

Using the approximation

$$C_{\text{effective}} = \frac{1}{\Delta V}\int_{V_1}^{V_2} C(v)\,dV = m.C(o)$$

where $C_{effective}$ is the effective depletion capacitance

$$C(v) = C(o) \quad (1 - \frac{V}{\phi_B})^{-\frac{1}{2}}$$

C(v) depletion capacitance as a function of applied voltage

V and C(o) is the zero bias depletion capacitance

$$C_{effective} = \frac{1}{V_2 - V_1} \; C(o) \int_{V_1}^{V_2} (1 - \frac{V}{\phi_B})^{-\frac{1}{2}} \, dV$$

$$= \frac{-2\phi_B \, Co}{V_2 - V_1} \left[(1 - \frac{V}{\phi_B})^{\frac{1}{2}} \right]_{V_1}^{V_2}$$

for emitter base junction, $V_2 \simeq .8\phi_B$ and V_1 is zero. In which case

$$C_{effective} \simeq 1.3 \, C_{eb}(0)$$

The collector base capacitance moves through twice the logic swing assuming a transition from $-.8\phi_B$ to $0.8\phi_B$. Using the above treatment but separating the integral into components $-.8\phi_B$ to zero and zero to $.8\phi_B$ the effective depletion capacitance as derived from change in stored charge on the collector base junction is:

$$2.3 \, C_{cb}(0)$$

Substituting into equation 4.6.

$$t_{de} \simeq \frac{V_{be} \, \beta_u}{C_b(\beta_u - 1)} \left\{ .65 \, C_{eb(0)} + (1 + n + m - \frac{m}{\beta_u}) \; 1.15 \, C_{cb}(o) \right\}$$

4.7.

i_b

In Chapter 2 expressions were derived for the power consumption of a I^2L gate in the on and off state. Assuming a system in which an equal number of gates are in each state, then the average power consumption P is (transient power is assumed zero)

$$P = \frac{1}{2} \text{ (Power on } + \text{ Power off)}$$

From Chapter 2

Power consumption of a gate switch in the 'off' condition =

$$V_{inj} \cdot I_{11}$$

Power consumption of a gate switched on =

$$V_{inj} \cdot I_{11} \left(1 - \frac{\alpha_n \alpha_i ((n+1) - n\alpha_d)}{1 - n\alpha_d \alpha_u}\right)$$

If V_{inj} for both cases is invariant the average power consumption P is

$$P = V_{inj} \cdot I_{11} \left(1 - \frac{\alpha n \alpha i((n+1) - n\alpha_d)}{2(1 - n\alpha_d \alpha_u)}\right) \qquad 4.8.$$

The base current of the I^2L gate is $\alpha_n I_{11}$. Combining equations 4.7 and 4.8 gives the power delay product $P \cdot D$ of an I^2L gate is:-

$$P \cdot D = \frac{V_{be} V_{inj} \beta u}{\alpha_n (\beta u - 1)} \left\{.65 C_{eb}(o) + (1 + n + m - \frac{m}{\beta u}) 1.15 C_{cb}(o)\right\}$$

$$\cdot \left\{1 - \frac{\alpha n \alpha i ((n+1) - n\alpha_d)}{2(1 - n\alpha_d \alpha_u)}\right\} \qquad 4.9.$$

Simplification of 4.9 is obviously possible with detailed knowledge of a given process.

The simple case switching of the I^2L gate in the regime dominated by depletion capacitance charge storage has been described. An expression for gate delay has been developed,

This expression shows gate delay to be simply dependent on depletion capacitance and the available base current. Power delay product is minimised by maximising the pnp α n.. The expression 4.9. shows that power delay product increases as V_{be} and V_{inj} increase. Thus even if other parameters are constant, power delay product increases with speed of operation.

4.5.2. Switching in constant delay region (Intrinsic delay)

The maximum gate delay of the I^2L device is limited by minority carrier storage effects in the epitaxy. A reasonable understanding of I^2L switching in this regime is possible using a charge control technique. (See ref. 38, p 327 for an introduction to charge control analysis). For this analysis the gate delay is divided into the following components

t_r rise time, time for devices to switch from off state to the edge of saturation.

t_s storage time, time to remove all stored charge in the device when switching gate off. Switching the gate from saturation to the edge of active operation.

t_f fall time, time to switch gate from the edge of active region to off state.

(no page 111)

Consider the switching cycle of T_1 Figure 4.3. at t = o a base current i_b is applied to its base. The collector current of T_1 = o at t = o. After the risetime period t_r the base current of $T_1 = i_b$ but now its collector current $I_c = i_b$, as the injector pnp of T_2 is identical to that of T_1. The device (T_1) is now saturated, if switch-off of T_2 commences. This is the beginning of the storage time interval t_s. At the beginning of the storage time period $I_c = i_b$ at the end of this period $I_c = \frac{i_b}{\beta u}$.

For the fall-time the initial collector current is $\frac{i_b}{\beta u}$ and the final is zero.

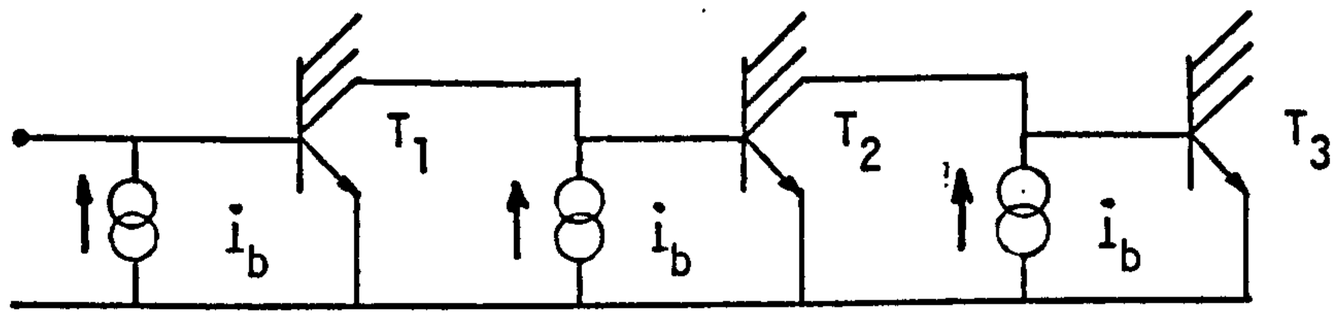
In conventional downward transistors the emitter stored charge is neglected. However, in I^2L the epitaxy stored charge is in the emitter of the upward operated device. Although this stored charge is in the emitter of the device it is important to realise that it is a consequence of base current, and can thus be incorporated into the total base current.

The following charge control relationship are assumed

$$\gamma_E = \frac{Q_B}{I_E}$$

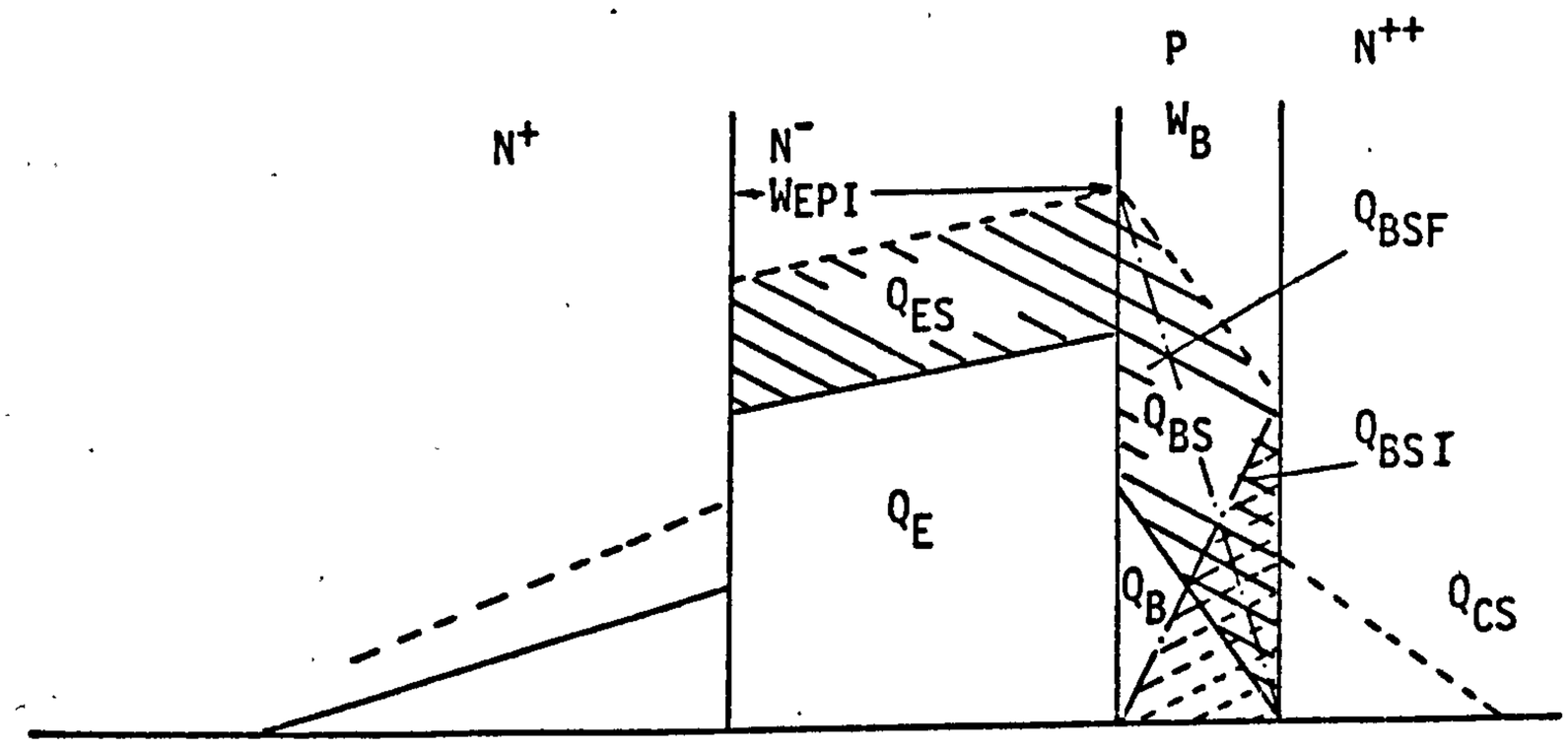
$$\gamma_B = \frac{Q_B}{I_B}$$

$$\gamma_C = \frac{Q_B}{I_C}$$



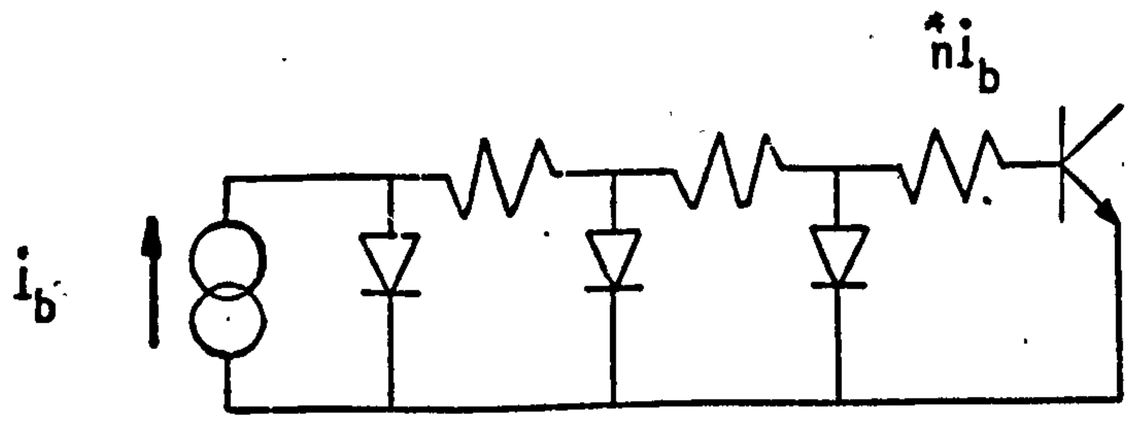
Circuit used to calculate intrinsic gate delay.

FIGURE 4.3



Minority carrier storage in saturation.

FIGURE 4.4



Equivalent circuit I^2L gate.

FIGURE 4.5

Q_B - stored charge associated with the base of the device

τ - time constant with subscript denoting region and the basic charge control relationship is

$$I = \frac{dQ}{dt} + \frac{Q}{\tau}$$

Rise time t_r

$$i_b = \frac{dQ_T}{dt} + \frac{Q_B}{\tau_B}$$ Q_T total charge storage in device

manipulating and multiplying by d I_c

$$\frac{d\,I_c}{i_b - \frac{Q_B}{\tau_B}} = \frac{1}{\frac{dQ_T}{dI_c}} \cdot dt$$

integrating for limits set for risetime described earlier

$$\int_0^{I_c} \frac{dI_c}{i_b - \frac{Q_B}{\tau_B}} = \int_0^{t_r} \frac{i}{\frac{dQ_T}{dI_c}} \cdot dt$$

noting that $\frac{Q_B}{\tau_B} = \frac{I_c}{\beta_u}$ and that $\frac{dQ_T}{dI_c} = \frac{i}{\omega_T}$

$$\int_0^{I_c} \frac{dI_c}{i_b - \frac{I_c}{\beta u}} = \int_0^{t_r} \omega_T \, dt$$

at the end of the rise time period $I_c = i_b$ in I^2L

Then $$t_r = \frac{\beta u}{\omega_T} \ln \frac{\beta u}{\beta u - 1} \qquad 4.10$$

Storage times t_s

In saturation the collector base and emitter base junctions are forward biased, This results in an excess charge being stored in the device. Further as the effective gain of the device has been reduced due to the action of the now operating inverse transistor the V_{be} on the emitter base of the device is increased in order that the collector may sink the full load current. In normal planar devices (downward mode) the forward biasing of the collector junction in saturation results in a significant charge being produced in the collector body. This region is usually relatively lowly doped. In I^2L operation the conventional regions have been transposed. The forward biasing of the collector (emitter diffusion) which is heavily doped results in only a small addition to the total stored charge. The major increase in the stored charges occurs in the epitaxy and base regions.

Figure 4.4. shows schematic representation of the minority carrier densities in the saturated I^2L device. In areas of base with no collectors. excess electrons

are stored. However, in most cases of interest only the low doped region of the epitaxy are of significance for minority carrier storage because:

1) Volume of this region is large in comparison to other charge storage regions

2) Minority carrier densities are inversely proportional to doping levels and epitaxy is the lowest doped region.

It should be noted that the charge stored in the base of the lateral pnp injector transistor is the next most significant minority carrier storage, as the region has similar doping to the epitaxy beneath the base land. The volume of this region is smaller than that of the low doped epitaxy, but it may become significant in I^2L structures with very thin epitaxy.

If Q_E and Q_B are the emitter and base charges necessary

to bring the device to the edge of saturation and Q_{ES}, Q_{BS} and Q_{CS} are the total stored charge in the device in the emitter base and collector regions respectively in saturation then Q_{BX}, the excess stored charge is given by

$$Q_{BX} = Q_{ES} + Q_{BS} + Q_{CS} - (Q_E + Q_B)$$

Storage time t_s is the time to reduce Q_{BX} to zero. If I_{B1} is the base current necessary to maintain the device in saturation and I_B^* is the base current necessary to bring the device to the edge of saturation, then the excess base current in saturation I_{BX} is given by

$$I_{BX} = I_{B1} - I_B^*$$

γ_s the storage time constant is then

$$\gamma_s = \frac{dQ_{BX}}{d\,I_B} \simeq \frac{Q_{BX}}{I_{BX}}$$

Dividing Q_{BS} into components Q_{BSF} and Q_{BSI} due to forward and inverse actions of the device

$$Q_{TOTAL} = Q_{BSF} + Q_{ES} + Q_{BSI} + Q_{CS}$$

Q_{BSF} and Q_{ES} correspond to the stored charge in the forward direction as a result of saturation and Q_{BSI} and Q_{CS} correspond to the stored charge in the inverse direction as a

result of saturation. The forward emitter current associated with Q_{BSF} and Q_{ES} is I_F and the inverse current associated with Q_{BSI} and Q_{CS} is I_I

$$I_I = I_{Ip} + I_{In}$$

I_{In} is electron current injected into the base

I_{Ip} is hole current injected into the collector

$$\gamma_s \simeq \frac{Q_{BX}}{I_{BX}} = \frac{(Q_{ES} + Q_{BSF}) + Q_{BSI} + Q_{CS} - (Q_B + Q_E)}{I_{BX}}$$

substituting for time constants γ_E, γ_B and γ_C as defined initially

$$\gamma_s \simeq \frac{Q_{BX}}{I_{BX}} = \frac{1}{I_{BX}} \quad (\gamma_E I_F + \gamma_{EI} \; I_{In} + \gamma_{CS} \; I_{IP})$$

γ_{EI} is inverse emitter time constant.

Sunstituting α_d for inverse common base gain and α_u for forward common base gain

$$\alpha_d = \frac{I_{In}}{I_{In}+I_{Ip}} = \frac{I_{In}}{I_I}$$

$$I_{In} = \alpha_d \, I_I$$

$$I_{Ip} = (1 - \alpha_d) \, I_I$$

$$I_{B1} = (1 - \alpha_u) \, I_F + (1 - \alpha_d) \, I_I$$

$$I_B^* = (1 - \alpha_u) \, I_E$$

$$I_{BX} = (1 - \alpha_u)(I_F - I_E) + (1 - \alpha_d) I_I$$

$$I_C = \alpha_u \, I_E = \alpha_u \, I_F - I_I$$

$$I_F - I_E = \frac{I_I}{\alpha_u}$$

$$I_{BX} = \frac{(1 - \alpha_u) I_I}{\alpha_u} + (1 - \alpha_d) I_I$$

$$= \frac{I_I}{\alpha_u} (1 - \alpha_d \alpha_u)$$

$$\gamma_s = \frac{\alpha_u}{I_I(1-\alpha_d\alpha_u)}\left\{\gamma_E I_F + \gamma_{EI}\alpha_d I_I + \gamma_{CS} I_I (1-\alpha d) - \gamma_E I_E\right\}$$

$$= \frac{\alpha_u}{I_I (1-\alpha_d \alpha_u)}\left\{\gamma_E \frac{I_I}{\alpha u} + \gamma_{EI}\alpha d I_I + \gamma_{CS} I_I (1-\alpha d)\right\}$$

$$= \frac{\gamma_E + \gamma_{EI}\alpha_u \alpha_d}{(1-\alpha_d \alpha_u)} + \frac{\alpha_u (1-\alpha_d)\gamma_{CS}}{(1-\alpha_d \alpha_u)} -$$

For the I^2L device the time constant of the collector is that of the downward emitter and as this region has a low volume and a high doping little minority carrier storage takes place. The downward cut-off frequency of planar transistors is usually in excess of several hundred megahertz, and therefore γ_{CS} must be small and can be neglected in the expression for γ_s.

Also we can make the assumption that the time constants γ_E and γ_{EI} are nearly equal, as both relate to stored emitter charge in the low doped epitaxy region. We can write therefore:

$$\gamma_s \simeq \gamma_E \frac{(1+\alpha_u \alpha_d)}{(1-\alpha_u \alpha_d)} \qquad 4.11$$

Now, in the storage time interval

$$I_B = \frac{Q_B}{\gamma_B} + \frac{Q_{BX}}{\gamma_s} + \frac{dQ_B}{dt} + \frac{dQ_{BX}}{dt}$$

s

and, the storage time interval ends when $Q_{BX} = 0$. In this time interval $\frac{dQ_B}{dt} = 0$ by definition. In I^2L a gate in saturation is switched off by a previous I^2L gate. In figure 4.3 assume that T_1 is switched on abruptly and in turn switches off T_2, the collector T_1 draws a current $\beta_u i_b$ and the injector of T_2 is continuously supplying i_b.

Thus the net current removed from the base of T_2 is

$$-(\beta_u - 1)\, i_b$$

$$\therefore \quad i_b (1 - \beta u) = \frac{Q_B}{\tau_B} + \frac{Q_{BX}}{\tau_s} + \frac{dQ_{BX}}{dt}$$

$$= \frac{I_C}{\beta u} + \frac{Q_{BX}}{\tau_s} + \frac{d_{QBX}}{dt}$$

$$\frac{dQ_{BX}}{dt} = i_b (1 - \beta_u) - \frac{I_C}{\beta_u} - \frac{Q_{BX}}{\tau_s}$$

taking reciprocals, multiplying by dI_{BX} and integrating over the storage time interval we obtain

$$\int_0^{t_s} \frac{1}{\frac{dQ_{BX}}{dI_{BX}}}\, dt = \int_{i_b - \frac{i_b}{\beta_u}}^{0} \frac{dI_{BX}}{i_b (1 - \beta u) - \frac{I_C}{\beta_u} - \frac{Q_{BX}}{\tau_s}} \qquad 4.12$$

$\frac{i_b}{\beta_u}$ is base current at the edge of saturation.

I_{BX} is the excess base current flowing in the storage time interval

$$\frac{dQ_{BX}}{I_{BX}} = \gamma_s$$

By charge control definitions in storage time interval the excess base current is as follows:

$$\frac{Q_{BX}}{\gamma_s} = I_{BX}$$

Substituting into 4.12 and integrating (noting that $I_C = i_b$ in I^2L)

$$t_s = \gamma_s \ln \frac{\beta_u 2}{(\beta_u^2 - \beta_u + 1)} \qquad 4.13$$

Equation 4.11 gives an approximate expression for γ_s if we put $\alpha_d = 1$. In real structures this is justified since an overestimate error of less than 10% is introduced into the storage time constant. That is storage time constant is less than that calculated. For most purposes this is acceptable. We can write an approximate expression for t_s:

$$t_s = \gamma_E \frac{(1+\alpha_u)}{(1-\alpha_u)} \ln \frac{\beta_u^2}{(\beta_u^2 - \beta_u + 1)}$$

Using the relationships

$$\gamma_E = \frac{Q_B}{I_E} \qquad I_E = \frac{I_C}{\alpha_u} \qquad \gamma_C = \frac{Q_B}{I_C}$$

$$\gamma_E = \alpha_u \gamma_C$$

and $t_s = \gamma_C \beta_u (1 + \alpha_u) \ln \frac{\beta_u^2}{(\beta_u^2 - \beta_u + 1)}$

To first approximation $\gamma_c = \frac{1}{\omega_T} \left(\simeq \frac{Q}{I_c} \right)$

Hence $$t_s = \frac{\beta_u}{\omega_T} (1 + \alpha_u) \ln \frac{\beta_u^2}{(\beta_u^2 - \beta_u + 1)} \qquad 4.14$$

Fall time t_f

The fall time if the I^2L gate may be calculated in a similar manner to the rise time. In the fall-time period the device is in active operation

$$I_B = \frac{Q_B}{\gamma_B} + \frac{dQ_B}{dt}$$

$$\frac{dQ_B}{dt} = I_B - \frac{Q_B}{\gamma_B}$$

Taking the reciprocal multiplying by dI_c and integrating

$$\int_0^{t_f} \frac{1}{\frac{dQ}{dI_c}} \cdot dt = \int_I^0 \frac{dI}{I_B - \frac{Q_B}{\gamma_B}}$$

$I_c = I_b$ in I^2L $\qquad \gamma_c = \frac{Q_B}{I_c} \qquad \frac{\gamma_c}{\gamma_B} = \frac{1}{\beta_u}$

$$\int_0^{t_f} \frac{1}{\frac{dQ}{dI_c}} \cdot dt = \int_{i_b}^0 \frac{dI}{I_b - \frac{I_c}{\beta_u}}$$

$I_b = -i_b (\beta_u - 1)$ as in storage time case

$$\frac{dQ}{dI_c} \simeq \frac{1}{\omega_T}$$

$$t_f = \frac{\beta_u}{\omega_T} \ln\left\{\frac{\beta_u^2 - \beta_u + 1}{\beta_u^2 - \beta_u}\right\} \qquad 4.15$$

Gate delay t_{di} is half the time taken to switch the device from on to off

$$t_{di} = \tfrac{1}{2} (t_r + t_s + t_f)$$

Combining 4.10, 4.14 and 4.15 gives:

$$t_{di} = \frac{\beta_u}{\omega_T} \ln\left\{\frac{\beta_u}{(\beta_u - 1)}\right\} + \frac{\beta_u}{2\omega_T} \ln\left\{\frac{\beta_u^2}{(\beta_u^2 - \beta_u + 1)}\right\} \qquad 4.16$$

4.5.3. Effect of base resistance on Intrinsic delay

The base of the I^2L gate can be represented as a distributed network (Figure 4.5). The base resistance results in a different high current gain characteristic for the collectors nearest and most remote from the injector (Chapter 3, Figure 3.17). This difference in gain affects the intrinsic delay of a collector on an I^2L gate.

If i_b is the base current injected by the injector then let the base current arriving at a collector remote from the injector be $\overset{*}{n}\, i_b$. Now that collector has to sink the whole of the base current of the gate it is driving for all the collectors of that gate to be switched off. Thus the

collector current for the collector with $n^* i_b$ base current must be i_b. Applying these conditions to the solution for gate rise time in the manner used to derive equation 4.10 results in the following for gate rise time

$$t_r = \frac{\beta_u}{\omega_T} \ln \frac{\beta_u}{\beta u - \frac{1}{n}} \qquad 4.17$$

The collector remote from the injector received less base current, therefore it is not so heavily saturated as the collectors near to the injector. Thus storage time is reduced.

For similar collectors on successive gates the storage time can be estimated as follows.

The base current arriving under a remote collector is ni_b and at the edge of saturation it is i_b/β_u. The net current removed from the saturated gate is ni_b minus the current demanded by the following gate's collector, $n^* i_b \beta u$. For similar gates the current removed is then

$$n^* i_b (1 - \beta u)$$

Equation 4.12 becomes

$$n^* i_b - \frac{i_b}{\beta u} \int_0^o \frac{d I_{BX}}{i_b n^* (1 - \beta u) - \frac{I_c}{\beta u}} - I_{BX} = \int_o^{t_s} \left\{ \frac{\frac{dt}{dQ_{BX}}}{\frac{dI_{BX}}{dI_{BX}}} \right\} \qquad 4.18$$

$$t_s = \frac{\beta_u}{\omega_T}(1+\beta u)\ln\left(\frac{\beta_u^2}{\beta u^2 - \beta u + 1/\overset{*}{n}}\right) \qquad 4.19.$$

In the fall time period the effective base current removed from a gate drive-in by a collector in a similar configuration is $n\, i_b (1-\beta u)$ as in the storage time case.

The fall time is then given as follows:

$$\int_0^{t_f} \frac{1}{\frac{dQ}{dI_c}}\,.dt = \int_{I_c}^{o} \frac{dI_c}{I_b - \frac{I_c}{\beta u}}$$

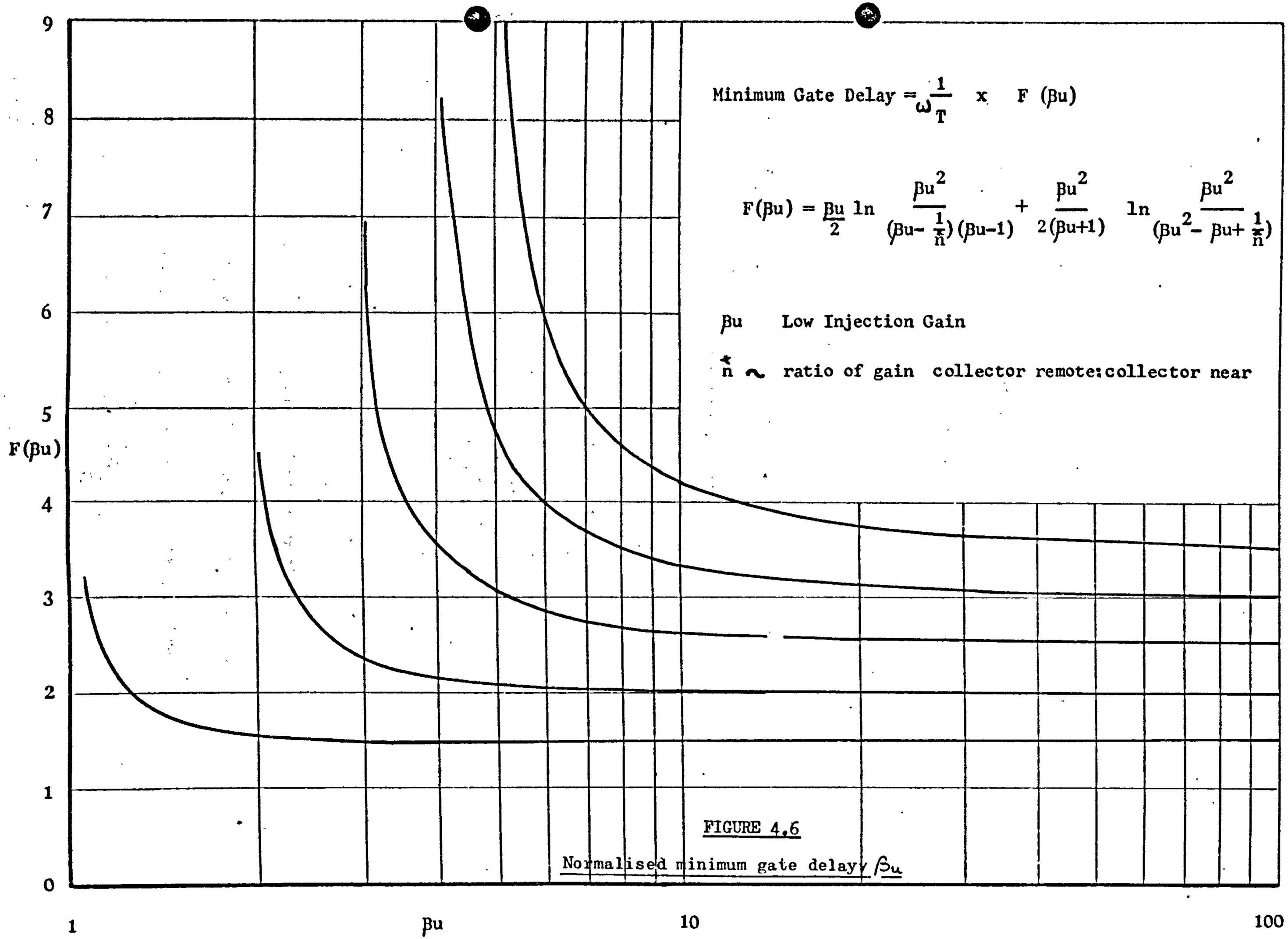
$$I_c = i_b \qquad I_b = \overset{*}{n} i_b (1-\beta u)$$

$$t_f = \frac{\beta u}{\omega_T}\ln\left\{\frac{\beta u^2 - \beta u + 1/\overset{*}{n}}{\beta u^2 - \beta u}\right\} \qquad 4.20$$

Combining equations 4.17, 4.19 and 4.20 gives the following for intrinsic delay

$$t_{di} = \frac{\beta_u}{2\omega_T}\ln\frac{\beta_u^2}{(\beta u - 1)(\beta u - 1/\overset{*}{n})} + \frac{\beta_u^2}{2\omega_T(\beta u+1)}\ln\frac{\beta_u^2}{(\beta u^2 - \beta u + 1/\overset{*}{n})} \qquad 4.21.$$

This expression (4.21) is plotted in Figure 4.6 (normalised to ω_T) for various values of $\overset{*}{n}$. To a first approximation, the ratio of the injected base current to the base current arriving at a collector can be estimated from the ratio of the measured gain of the collector under consideration to the



$$\text{Minimum Gate Delay} = \omega_T^{-1} \times F(\beta u)$$

$$F(\beta u) = \frac{\beta u}{2} \ln \frac{\beta u^2}{(\beta u - \frac{1}{\overset{*}{n}})(\beta u - 1)} + \frac{\beta u^2}{2(\beta u + 1)} \ln \frac{\beta u^2}{(\beta u^2 - \beta u + \frac{1}{\overset{*}{n}})}$$

βu Low Injection Gain

$\overset{*}{n}$ ~ ratio of gain collector remote:collector near

FIGURE 4.6

Normalised minimum gate delay v βu

gain of the collector nearest the injector. This assumes that the intrinsic gain of each collector is identical and the observed values of gain is due to the different amounts of base current arriving at the collectors, the first collector nearest the injector seeing all the base current.

As $\overset{*}{n}$ decreases, implying more debiasing, t_{di} increases. $\overset{*}{n} = 1$ corresponds to equation 4.16, i.e. no debiasing. The effect of debiasing becomes more significant as βu decreases. With low βu the device has long rise and fall times and short storage times. As βu increases rise and fall times tend to decrease and storage time increases. The I^2L gate suffers from R.C. charging delays associated with the distributed nature of the device. However, these effects appear small compared with effects associated with loss in effective gain (βu) due to debiasing.

Figure 4.6 indicates that t_{di} is insensitive to βu over a large range of βu values. This appears to be in contradiction to the results of Klaasen, Weidmann and Berger etc. which show t_{di} to increase with increasing βu.

The effect of modifications to βu on t_{di} is felt most

strongly through the consequent changes in ω_T. If β_u is increased by a reduction in any of the base current components the associated charge storage increases.

To first approximation take any component of base current

$$J = q D \left.\frac{dn}{dx}\right|_{x=0}$$ (i.e zero electric field)

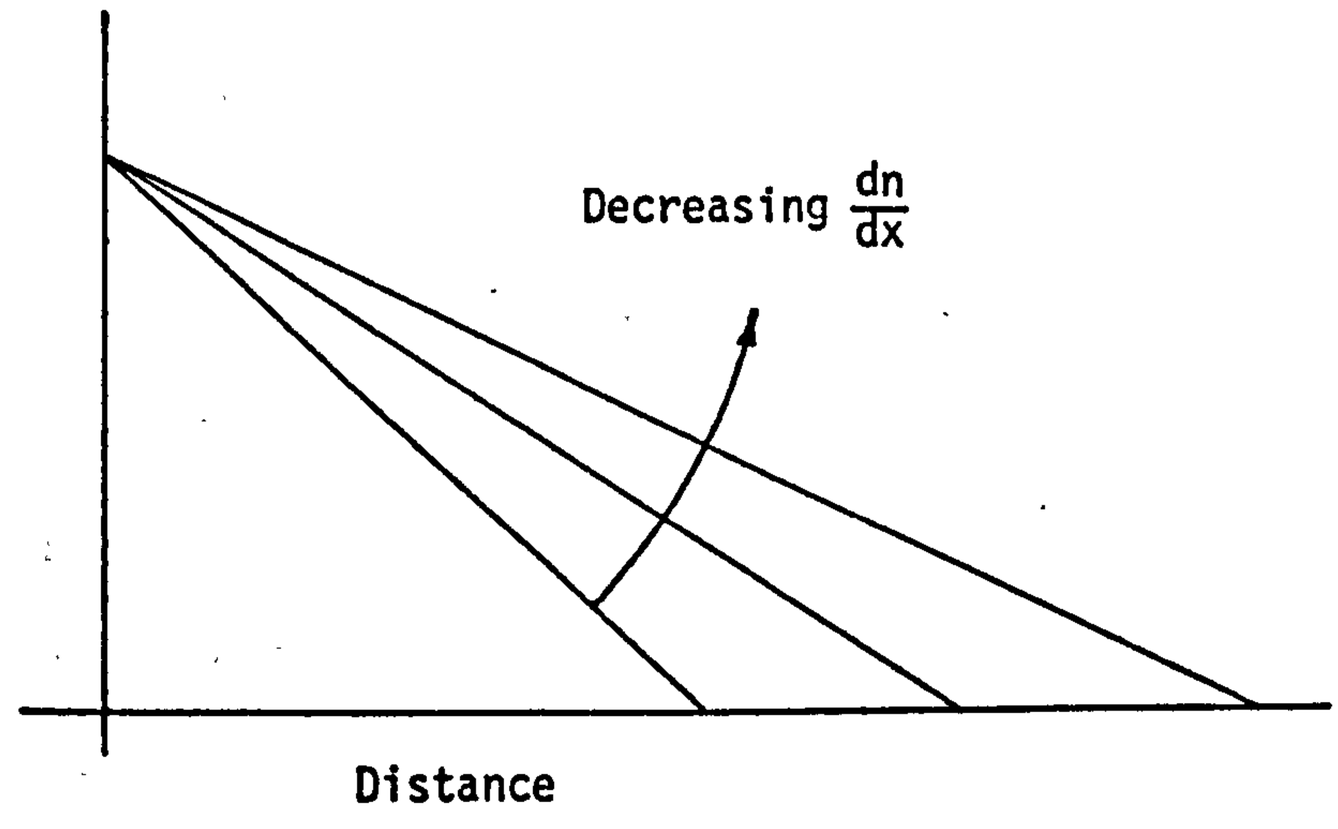
if $\frac{dn}{dx}$ is reduced, stored electrons increase (see Figure 4.7.)

β_u can be increased by reducing the intrinsic base integrated doping $\int N_B \, dx$

$$\omega_T \simeq \frac{dI_c}{dQ_T} \simeq \frac{I_c}{Q_T}$$

$$\simeq \frac{Ac}{A_B} \frac{Dn \; N_{D\,EPI}}{W_{EPI} \int N_B \, dx} \qquad 4.3.$$

Increasing β_u in this way increases ω_T and consequently decreases t_{di}.



Minority carrier storage.

FIGURE 4.7

These results are in close agreement with those quoted earlier, and the derived treatments are considerably easier to manage and give considerable physical insight into the switching operation of the I^2L gate. Figure 4.8 shows the calculated minimum gate delay (t_{di}), plotted against base buried N^+ clearance W_{EPI}, with β_d as a parameter for a Process III four collector I^2L gate.

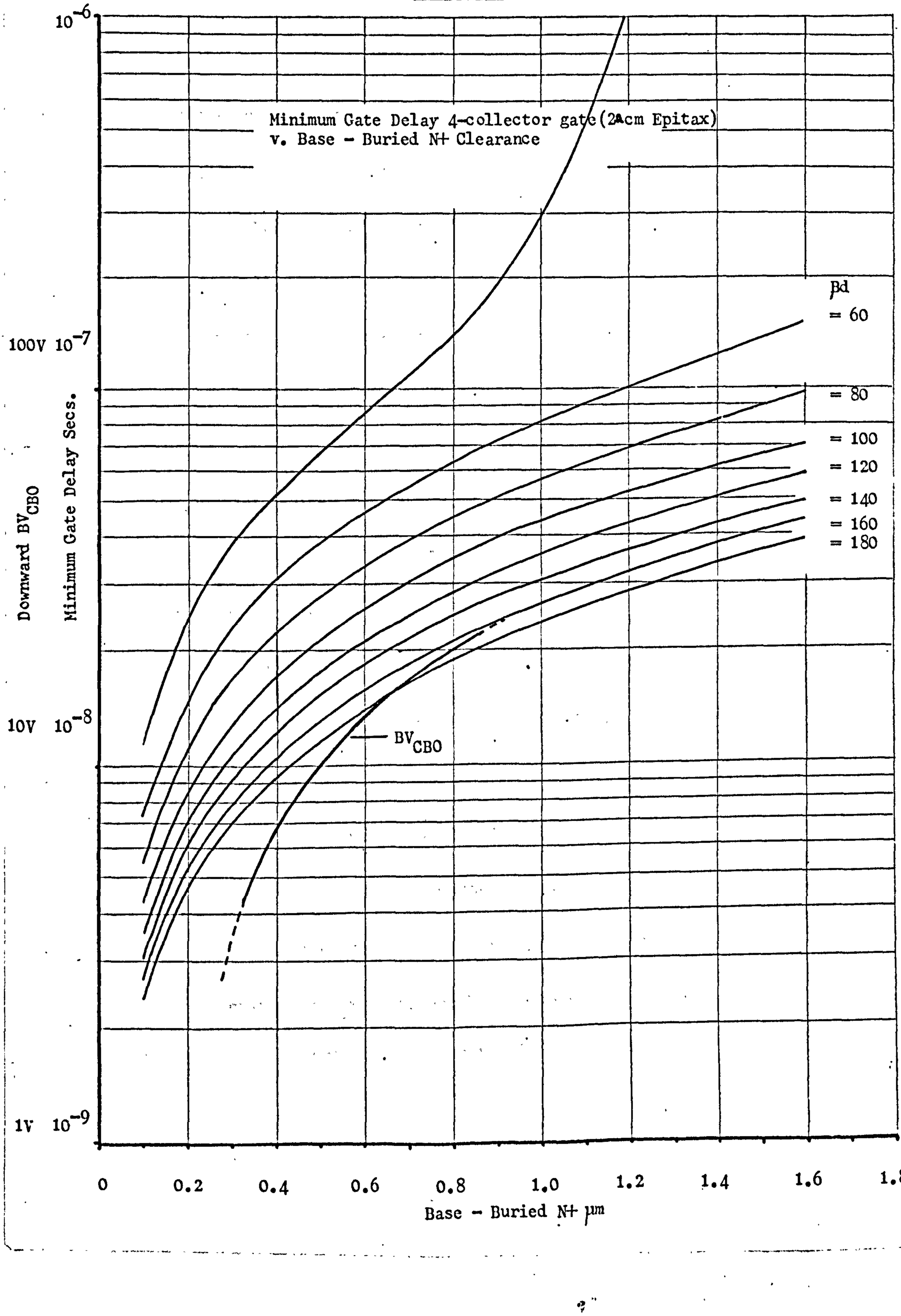
In Chapter 3 it was shown that βu could be calculated from βd and W_{EPI}. The delay is the calculated value for the collector nearest the injector, using equations 4.3. and 4.21.

Figure 4.8. has been found to have considerable experimental validity on Process III and has been observed to predict chip to chip variations across a single wafer.

The expressions also predict the behaviour of I^2L on the deep junction process, Process D.

In Chapter 6 it is shown that collector base breakdown voltage BV_{CBO} is dependent on base-buried N^+ clearance W_{EPI}. This relationship is shown on Figure 4.8. Thus βd and BV_{CBO} can be used to estimate t_{di} and also help to establish process compromises, such as whether a required breakdown voltage in the downward mode is compatible with a specified gate delay.

FIGURE 4.8,


Minimum Gate Delay 4-collector gate (2 cm Epitax) v. Base - Buried N+ Clearance
βd = 40
βd = 60
= 80
= 100
= 120
= 140
= 160
= 180
BV_{CBO}
Downward BV_{CBO}
Minimum Gate Delay Secs.
10^{-6}
100V 10^{-7}
10V 10^{-8}
1V 10^{-9}
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
Base - Buried N+ μm

DISCUSSION

The switching operation of the I^2L gate has been described in the constant power delay product and constant delay regimes. In the constant power delay product (t_{de}) regime (equations 4.7 and 4.9) delay is shown to be primarily dependent on depletion capacitance and injector pnp common base current gain. The smallest junction areas and narrowest pnp base width produce the lowest values of power delay product.

In the constant delay region (t_{di} equation 4.21) a high collector to base area ratio is required to minimise delay. The intrinsic delay requires a high βu and low base resistance for optimum performance. Thus the requirements for optimum power delay product and low intrinsic delay require certain compromises.

Decreasing junction areas tends to decrease junction area ratios A_C/A_B. A reduction in pnp base width will increase pnp α and reduce βu by increasing the lateral pnp re-injection current component of npn base current. Furthermore this will increase the frequency response, by reduction in

charge storage associated with the lateral re-injection. This is provided that βu does not fall below where F (βu) in Figure 4.6. increases. With the derived expressions it is thus possible to investigate the compromises for the implementation of I^2L on a particular process. These compromises include downward mode parameters such as β_d and BV_{CBO} and establish whether a set of requirements for power delay product, intrinsic delay, β d and BV_{CBO} are mutually exclusive. Thus one can decide whether a circuit requiring both I^2L and conventional components is feasible.

CHAPTER 5

EXPERIMENTAL OBSERVATIONS ON I^2L

5.1. INTRODUCTION

An extensive theoretical analysis of I^2L has been presented. We will now show how these treatments have real meaning and offer considerable insight into the operation of the I^2L in both DC and switching mode operation. The theory will be compared with experiment against a number of technologies which are significantly different. Details of the test masks used for these measurements are given in Appendices 4,5 and 6.

5.2. PROCESS III EXPERIMENTAL RESULTS

5.2.1. D.C. Operation

The basic Process III I^2L gate is shown in Appendix 1. The gate has 12 x 14 μm shallow n^+ diffusions acting as multiple collectors, and a 4 μm (as drawn) lateral pnp base width. Typical gain characteristics for a four collector gate are shown in Figure 5.1. The characteristics of the nearest and most remote collectors to the injector are detailed. The second and third collectors have characteristics between those shown.

The characteristic shows clearly the effect of debiasing between the first and most remote collector on the gate.

Weidmann and Berger structures (14) have been used to analyse the various components of injected current. The results for room temperature (20^oC) are shown in Figure 5.2.

In Chapter 3 it was stated that the downward gain β_d (see Figure 3.19).

EXPERIMENTAL βu v. I_B FOUR-COLLECTOR GATE

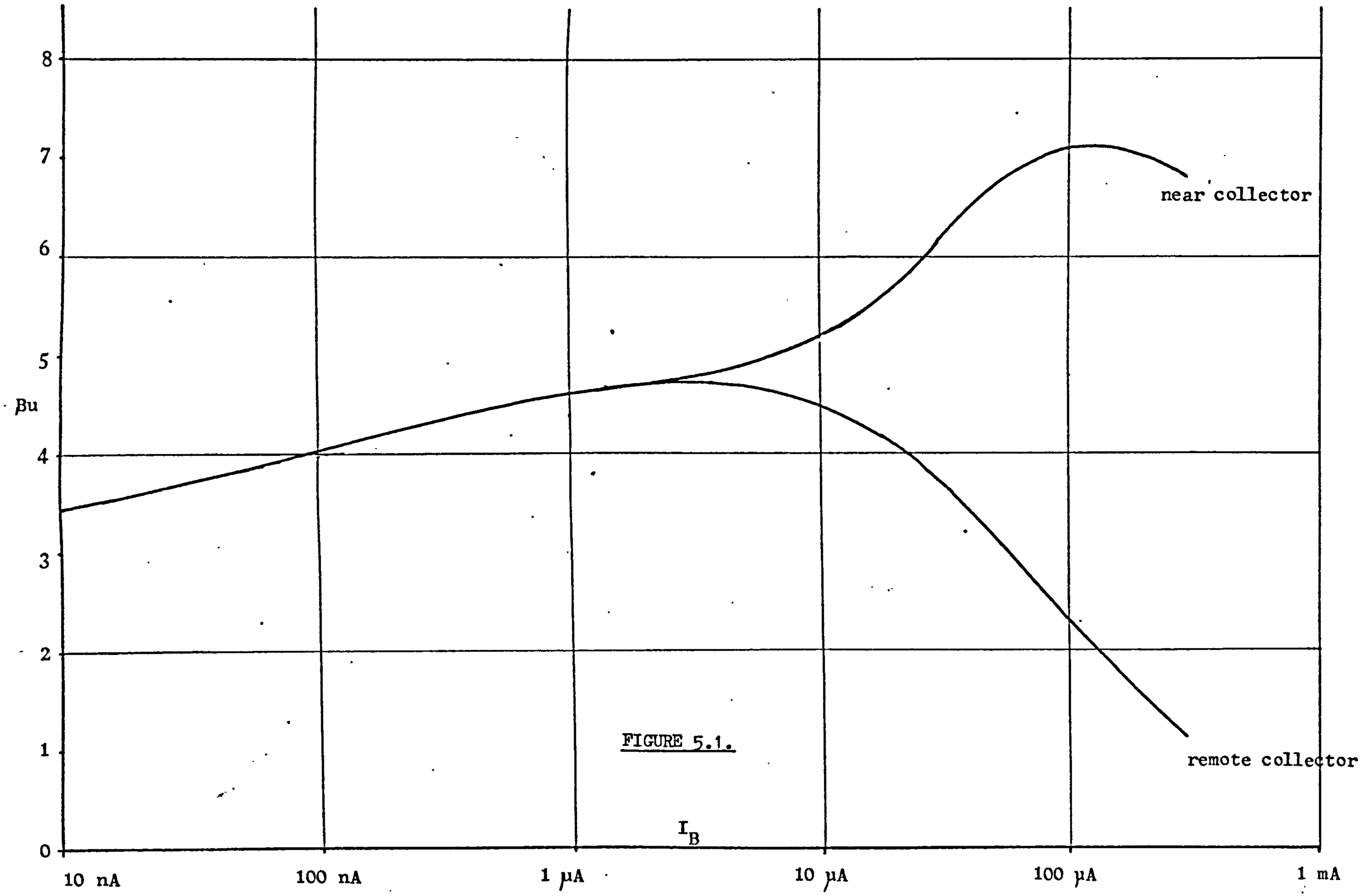


FIGURE 5.1.

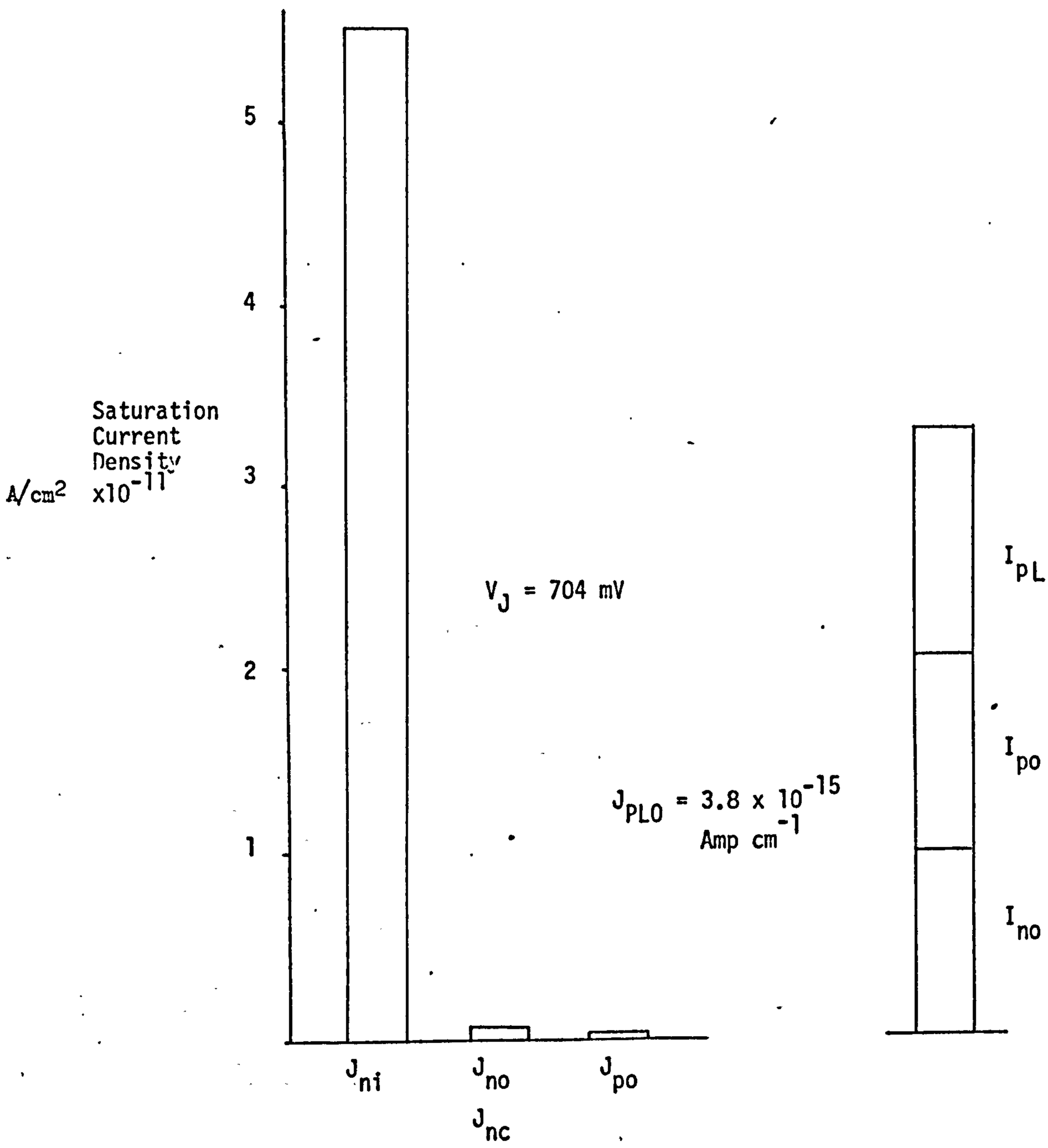
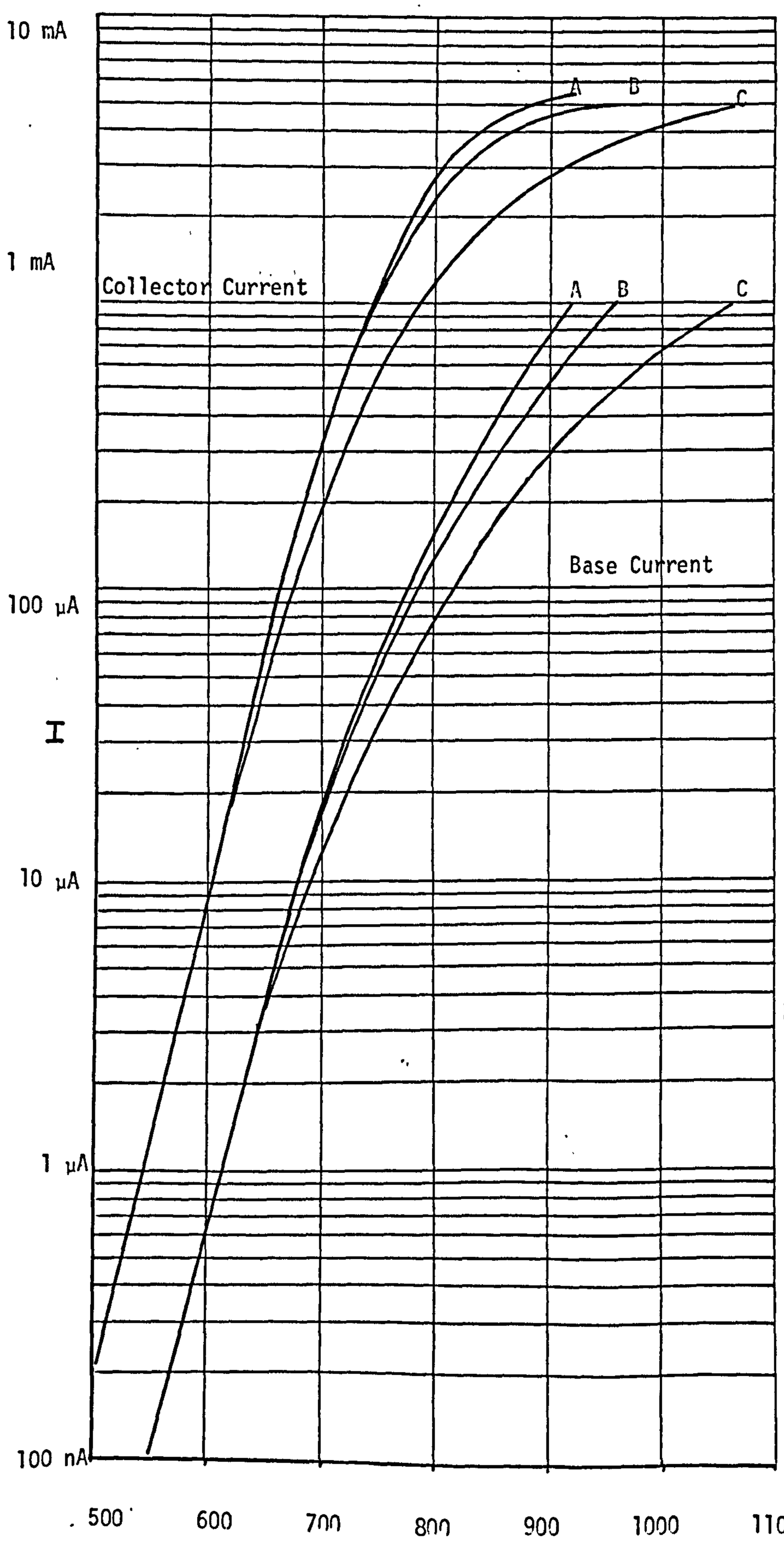


FIGURE 5.2

(a) Magnitude of injected saturation current densities

(b) 10 μA total base current portioned according to injection mechanism

FIGURE 5.3.



Process III I^2L Gate

4 Collectors in Parallel

Heidmann Berger Gate WT45

Downward BV_{CBO}

A 5Ω/sq. 25V

B 10Ω/sq. 20V

C 30Ω/sq. 23V

Lateral Re-injection

A 5Ω/sq. 613 mV 530nA

B 10Ω/sq. 613 mV 500nA

C 30Ω/sq. 613 mV 530nA

FIGURE 5.4.

Lateral pnp I_c, I_b V_{be} Characteristics (RL 20)

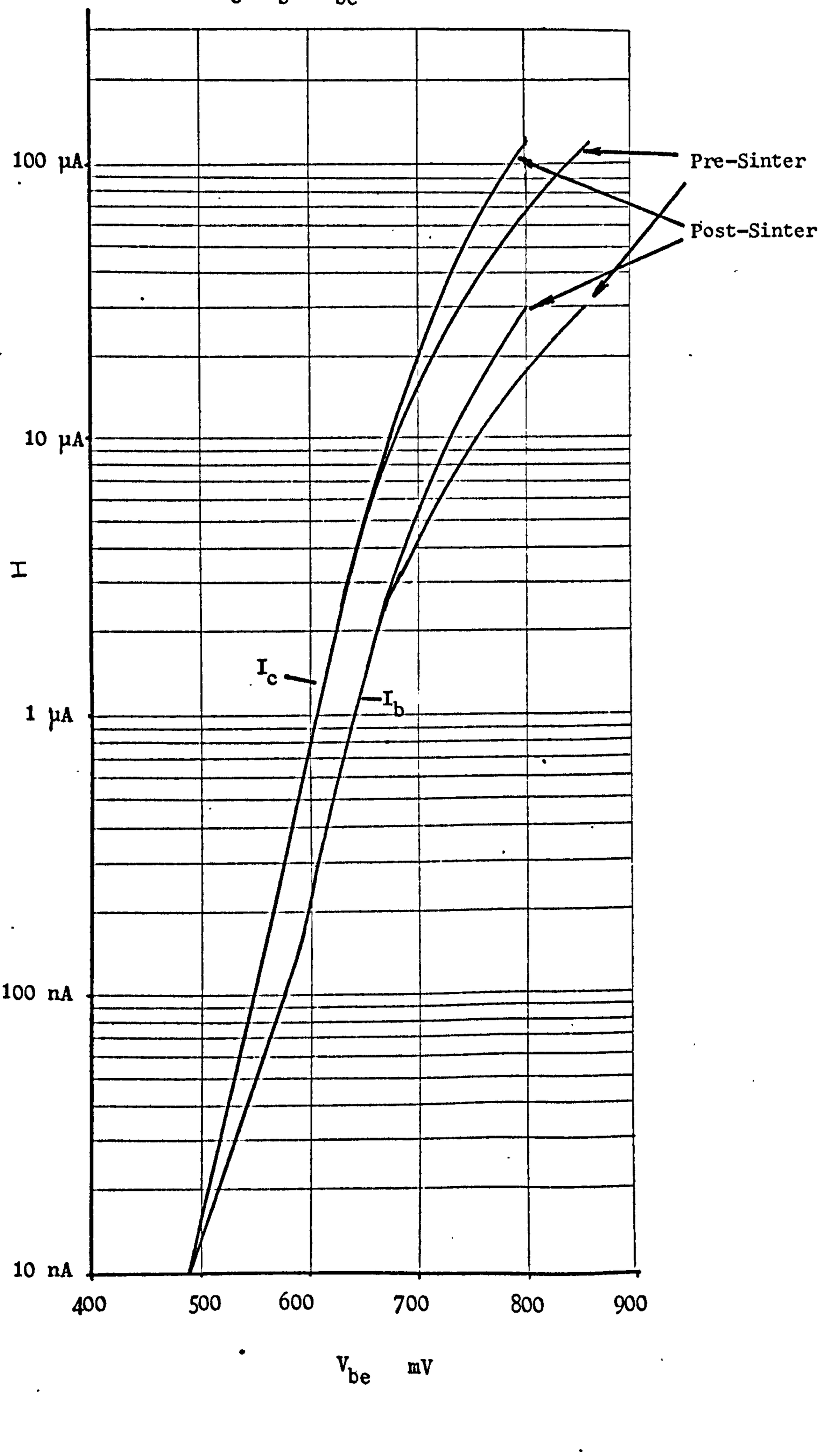


Table 5.1.

β_d	BV_{CBO}	β_u Expt.	β_u Calc.
50	10	1.7	1.65
80	6	2.5	2.1
100	7	4	3.6
120	15	3	3.7
180	8	6	6
250	10	8.5	8.7

Experimental values of β_d BV_{CBO} and β_u for various Process III batches.

This table of results is best understood if interpreted with figure 3.19.

BV_{CBO} is used to estimate the width of the low doped epitaxial region W_{EPI}.

β_d is a measure of integrated base doping (section 3.4). Thus β_u can be calculated from β_d and W_{EPI} if other parameters such as surface recombination velocity are considered invariant.

and BV_{CBO} could be used to predict βu in the medium injection regime. Table 5.1 lists experimental values of βu, βd and BV_{CBO} for various Process III batches, together with the calculated value of βu from βd and BV_{CBO}.

These results are in close agreement with the relationships predicted.

Various process modifications have been tried to improve βu. Several values of buried N^+ resistivity have been used (30, 10 and 5 ohms per square), thus changing total buried N^+ doping by a factor five. Careful analysis of these results (summarised in Figure 5.3) showed that only the I R drop associated with the resistance between the gate under test and the buried N^+ contact was modified.

The surface state density modifies the surface recombination velocity which is an important factor affecting transistor gain. Experiments to establish the optimum surface anneal/sinter at post metallisation, showed that a forming gas (10% H_2 in N_2) sinter at 425°C resulted in a significant low current gain improvement for the downward transistor, and an overall gain improvement for the upward transistor.

Unfortunately in Process III, the titanium/aluminium metallisation system does not naturally result in a reduction of surface recombination velocity, as in the aluminium system.

Figure 5.4. shows the I_c, I_b V_{be} characteristics of a lateral pnp in which the total transistor surface is covered by metallisation, thus denying the sinter/anneal ambient access to the silicon/silicon dioxide interface. However,

contact resistance is improved, thus reducing the high current V_{be}, Low current gain characteristics are unaltered by the sinter/anneal treatment.

Further aspects of device characterisation are given in Appendix 1. Sintering effects are further discussed in Chapter 7.

5.3. POWER DELAY PRODUCT MEASURED ON PROCESS III, RING OSCILLATOR.

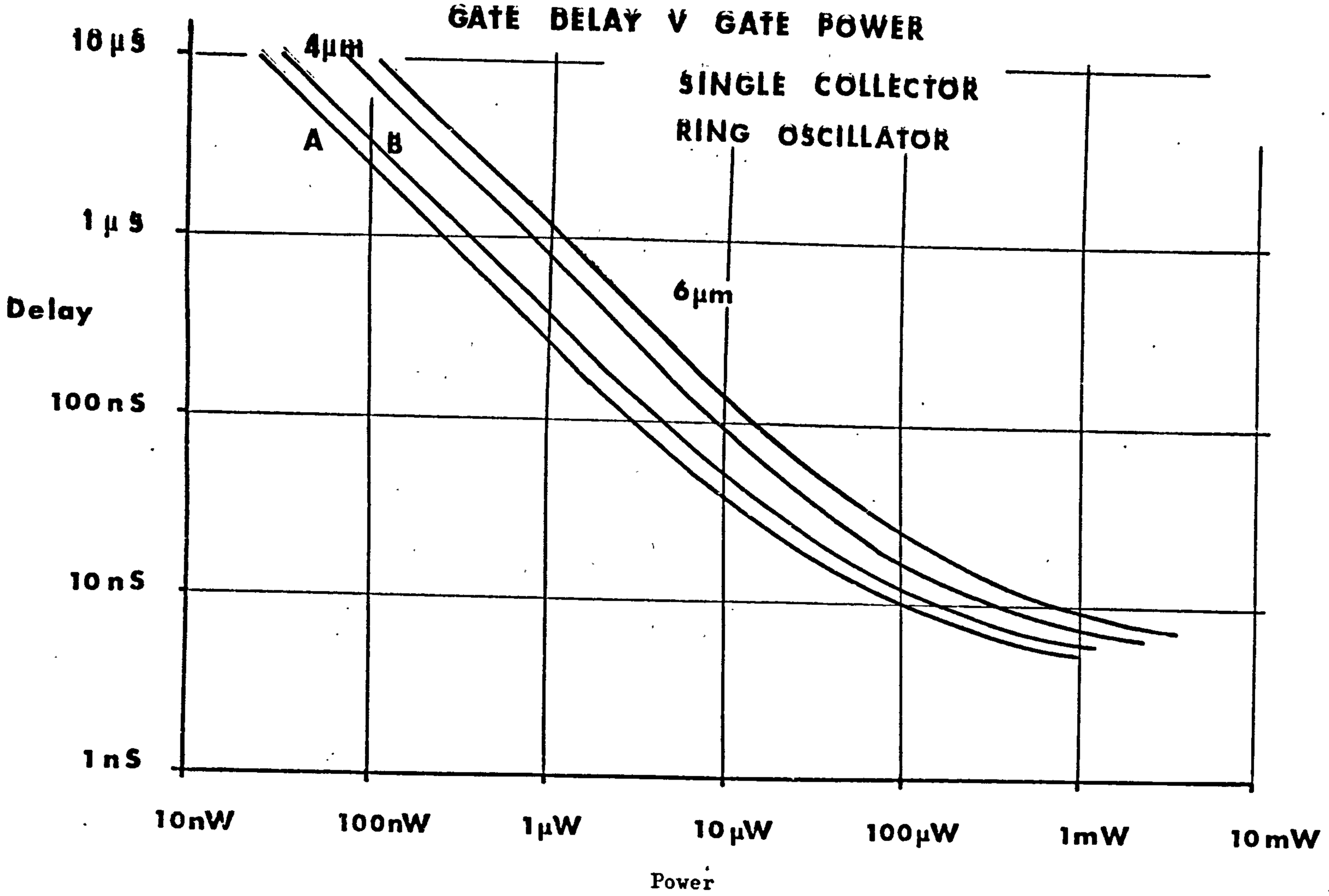
Ring Oscillators (odd number of inverters connected in a feedback ring) are not the ideal device for measuring the power delay product and minimum gate delay of any logic family. They usually represent the simplest logic function with minimum fan-in and fan-out. There is the danger that the full logic transition has not been made with a ring oscillator containing a small number of gates. Thus ring oscillators may give an optimistic figure of power-delay product and minimum gate delay. However, given these reservations the ring oscillator is still a very useful device and can readily yield information on such aspects of device operation, as geometry dependence of gate delay, and the dependence of gate delay on fan-out.

Very large ring oscillators (99 and 223 gates) have shown that the nine and seven gate ring oscillators give an accurate representation of gate delay, and the error due to incomplete logic swings is less than 5%.

5.3.1. Single Collector Ring Oscillators

Figure 5.5. shows measured power delay characteristics

FIGURE 5.5.


GATE DELAY V GATE POWER
SINGLE COLLECTOR
RING OSCILLATOR
10 µS
1 µS
100 nS
10 nS
1 nS
Delay
4µm
A
B
6µm
10nW
100nW
1µW
10µW
100µW
1mW
10mW
Power

for a single collector ring oscillator fabricated on Process III. The characteristics show the effect of changing lateral pnp base width which modified α_n and α_i. Reducing the lateral pnp base width increases α_n and α_i. In Chapter 4 it was shown that the power-delay product is proportional to $1/\alpha_n$. Minimum gate delay is determined by charge storage, and after the component due to epitaxy storage, the storage in the lateral pnp is the most significant component. Reduced pnp base width results in increased α_i and a reduction in charge storage. Thus reduced pnp base width results in both an improved power delay product and decreased minimum gate delay.

α_n and α_i can be maximised by extending the injector diffusion along the side of the base land as far as possible. These extensions are unmetallised and do not affect gate packing density. The additional characteristics in Figure 5.5 show a comparison of single collector ring oscillators with and without these interdigitated injectors (A and B respectively). These results clearly show the effect the injector pnp has on both power delay produced and minimum gate delay.

5.3.2. Multi collector Ring Oscillators

The single collector ring oscillator described the basic switching operation of the I^2L gate, however in order to implement logic using I^2L it is necessary to use a multi-collector

GATE DELAY V. GATE POWER

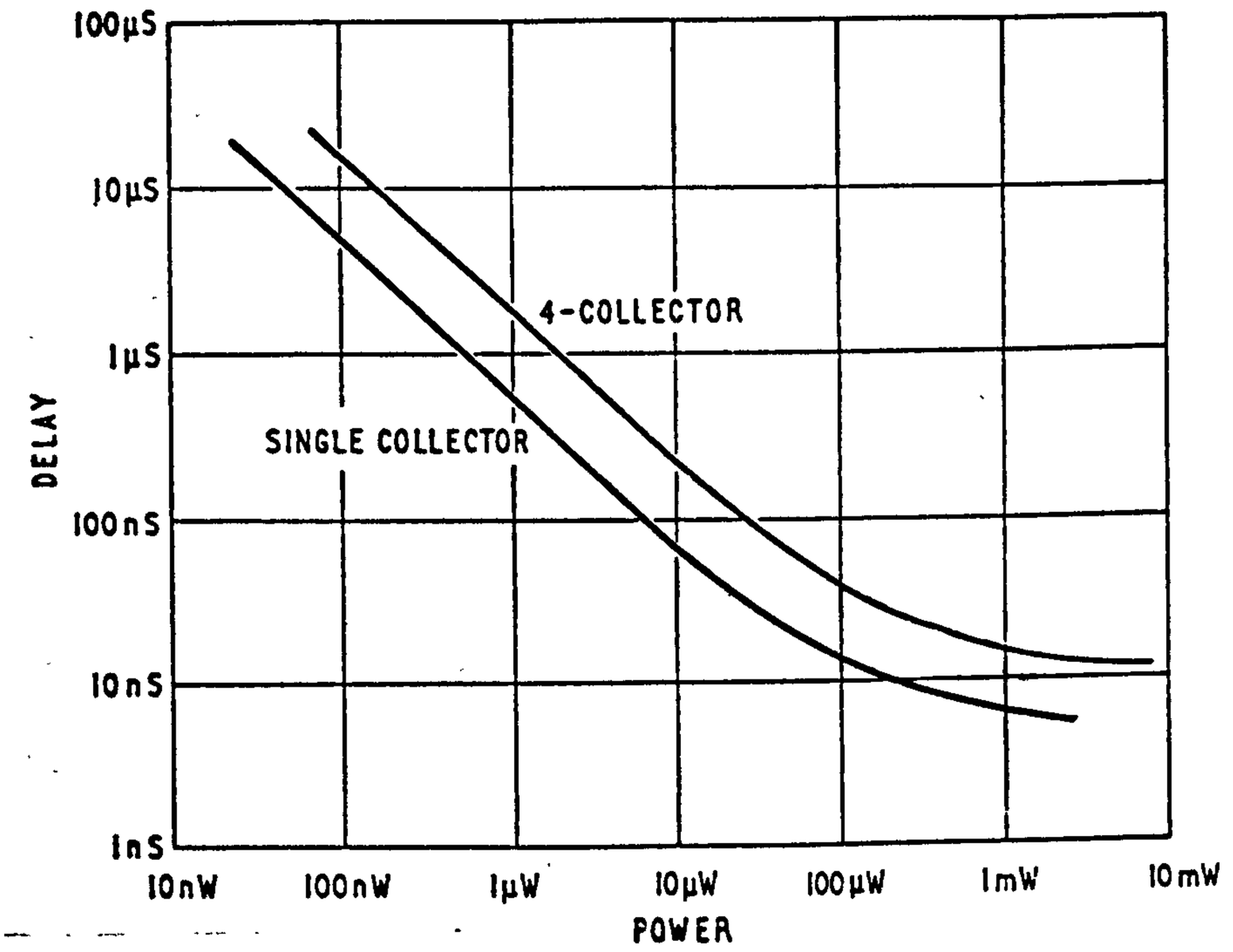


FIGURE 5.6.

gate. The following results show the effects of using a multi-collector gate.

In Chapter 4 the basic relationships controlling power delay product and minimum gate delay were established. The power delay product was shown to be dependent on the total depletion capacitance, which is controlled by gate area.

A two collector gate has approximately twice the base and collector area of a single collector gate, a three collector gate three times, and a four collector gate four times etc.

In Chapter 4 the minimum gate delay was shown to be dependent on the collector to base area ratio, stored charge being proportional to base area and collector current proportional to collector area. Figure 5.6. shows a comparison of a single and four collector ring oscillators from mask WT45 (see Appendix 3). The four collector device uses the collector nearest the injector and the base contact is adjacent to the injector on both devices. These experimental results clearly show the power delay product is proportional to gate fan out and minimum gate delay is proportional to the collector base area ratio.

5.3.3. Differential Gate delay on multi-collector gates

Experimental and theoretical evidence has been presented previously (Chapters 3,4, and 5) which shows the effect of debiasing on D.C. current gain of a multi collector

I^2L gate. The collector remote from the injector receives less drive than that nearest to the injector under conditions of large base current and hence has a smaller βu. βu effects switching performance of the I^2L gate as was shown theoretically in Chapter 4. Figure 5.7 shows the power delay characteristics for a number of four collector gate ring oscillators. The interconnection of the gates is shown in Figure 5.8. Case 1 is a ring oscillator with the base contact and collector adjacent to the injector. Case 2 is a ring oscillator with the base contact adjacent to the injector, and the feedback collector is the most remote from the collector. Case 3 is a ring oscillator with the base contact between the third and fourth (most remote) collector, and the remote collector is that in the feedback network. In Case 1 the collector has the highest gain as a result of *minimum* debiasing. Furthermore the base current of the following stage is extracted near to that current point of entry to the base land. This results in the whole base being switched in each transition. The second case shows the effect of debiasing of the base. The collector is required to sink the whole current entering the base land, whilst the debiasing has resulted in it receiving far less base drive at high currents

than the portion it received at low currents. As a result it takes a longer time to remove all the charge accummulated in the gate it is driving.

Injector current v gate delay 4-collector gate
(9-stage ring oscillator)

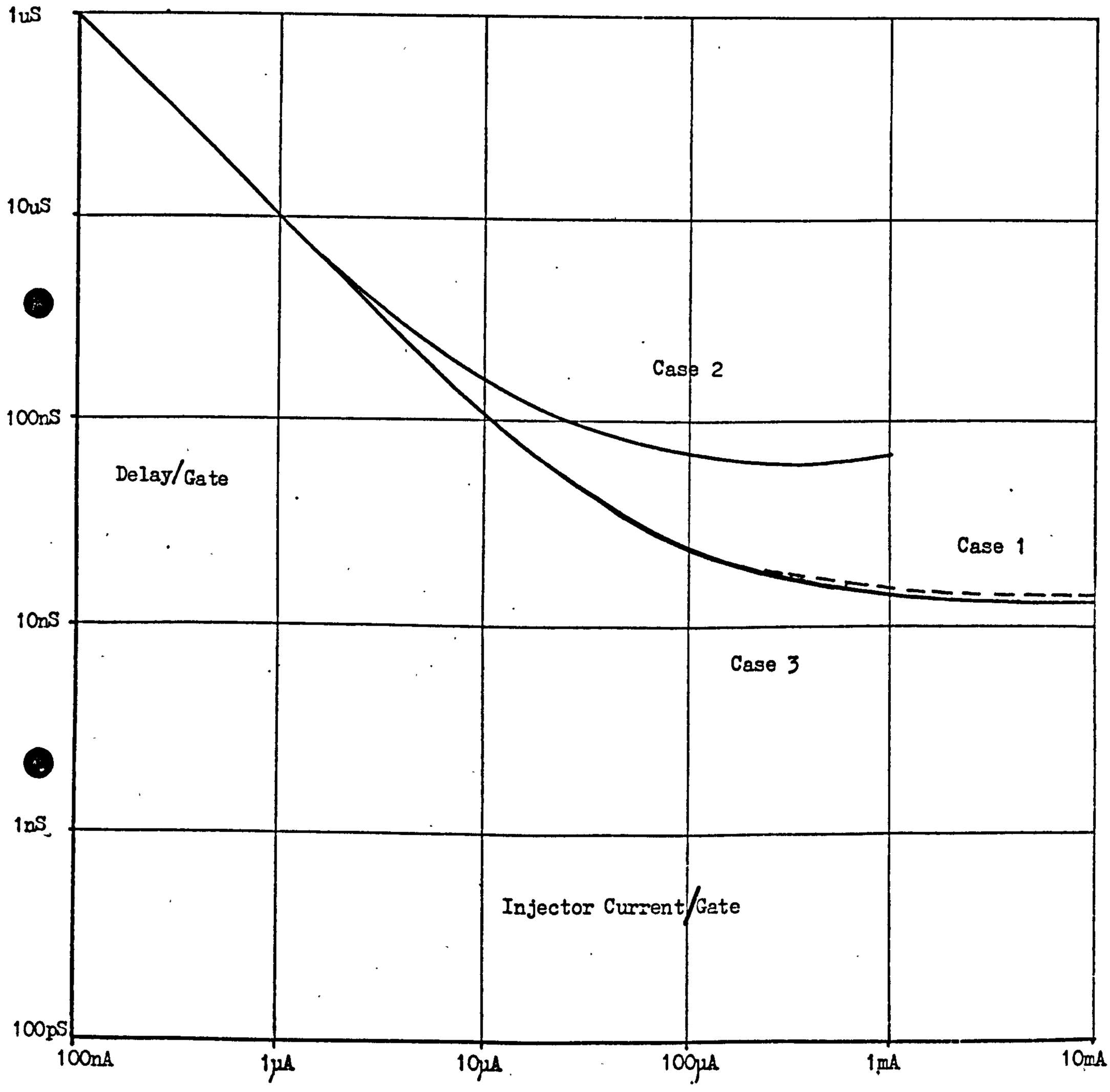


FIGURE 5.7.

On Process III this can result in a 5:1 ratio in minimum gate delay.

Case 3 produces an apparently surprising result. The power delay characteristic is essentially identical to that of Case 1. With the base contact located close to the remote collector, this collector is switched off as soon as the collector current in the previous gate reaches a value sufficient to sink the base current arriving at it, and does not need to wait for the charge in the whole of the preceeding gate to be removed. That is, the remote collector is switched off before the others. In this way the signal propagates at essentially the same speed achieved in Case 1. This is a consequence of debiasing. Although the structure oscillates, true I^2L action is not taking place since the collectors between the base contact and injector are capable of sinking part of a base current when the remote collector is turned off.

These results are in agreement with the theoretical predictions of Chapter 4.

This differential delay has serious consequences for synchronous systems, or where very high performance is required. There are several ways of mitigating this effect:

a) Arrange the gates alongside the injector (41).

This solution severely degrades packing density as logic interconnection becomes difficult.

b) Increase the width of the base land whilst maintaining the collector size. This is undesirable as it results in a significant reduction of upward f_t, which degrades the minimum gate delay and also reduces packing density.

A solution implementable on Process III is the previously described interdigitated injector I^2L gate. The injector may be extended down the entire length of the base land.

5.3.3. Multi-collector ring oscillators using Interdigitated Injector

Figure 5.8. shows a layout comparison of a standard and interdigitated injector four collector I^2L gate. Figure 5.9. shows simple equivalent circuit comparisons of the two techniques. This shows clearly that the base current is supplied via a distributed source in the interdigitated case.

The power-delay characteristics of ring oscillators fabricated using this technique are shown in Figure 5.10. The two cases of the collector nearest the main injector (Case 1) and that most remote from the main injector (Case 2) used in the feedback loop are compared. The base contact was adjacent to the main injector in both cases. The results are from devices from the same silicon slice as those presented earlier for standard multi-collector ring oscillators. The results show an improvement in power delay product over the standard structure as the α_n of the injector has been improved. The best case minimum gate

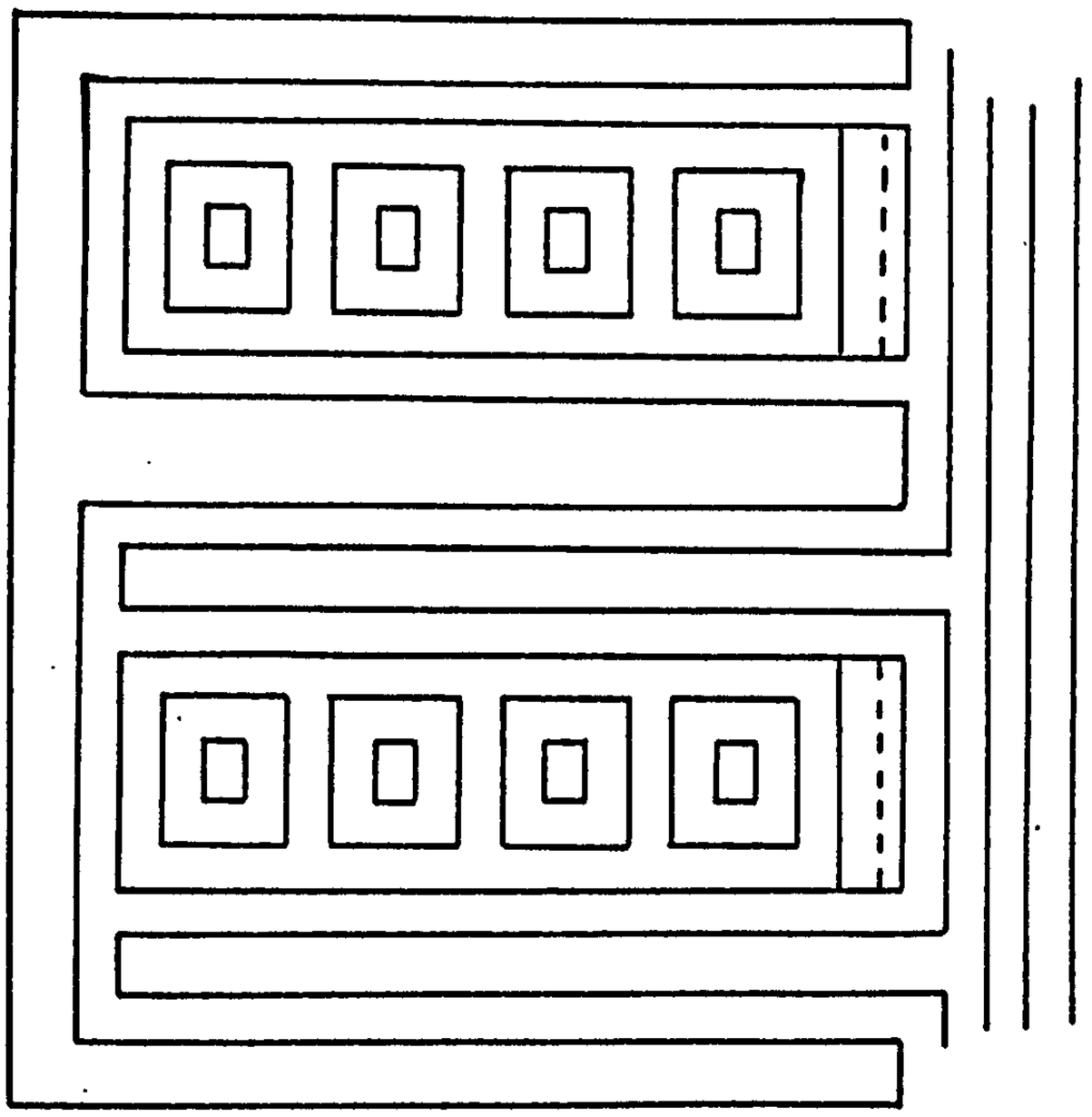
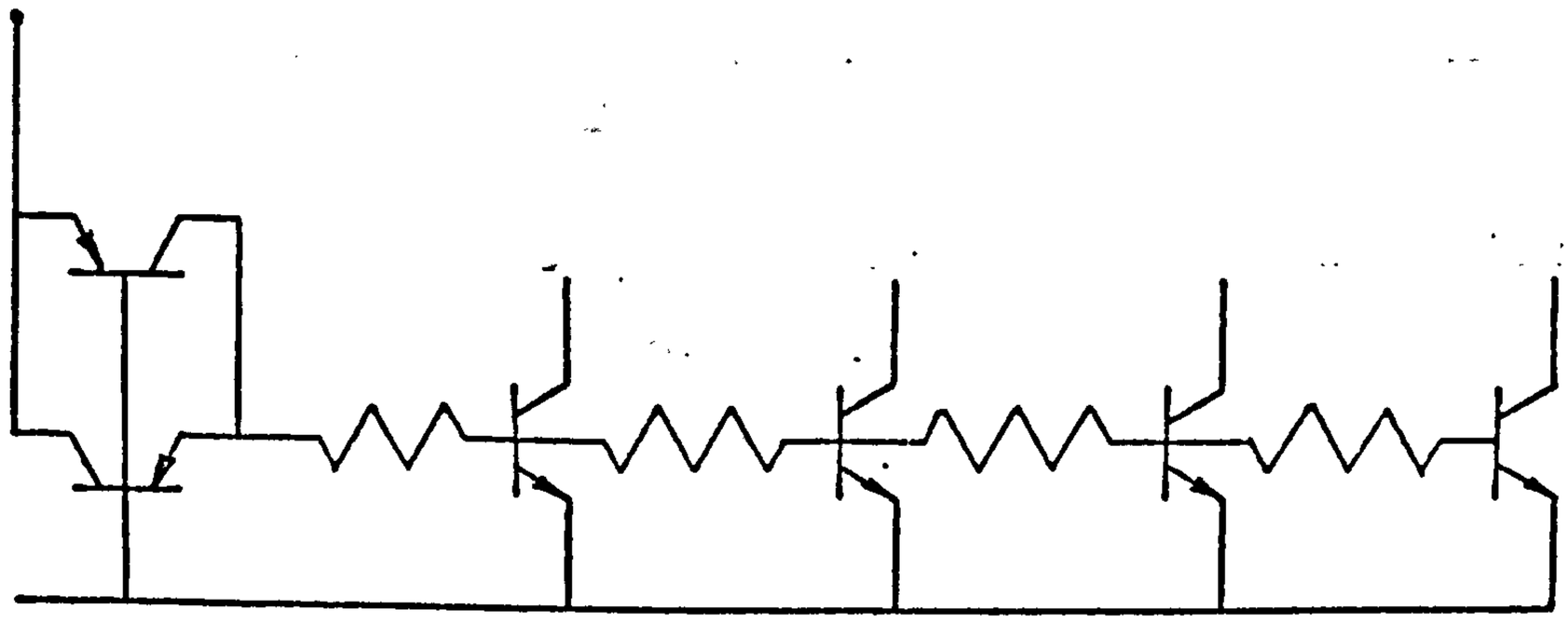
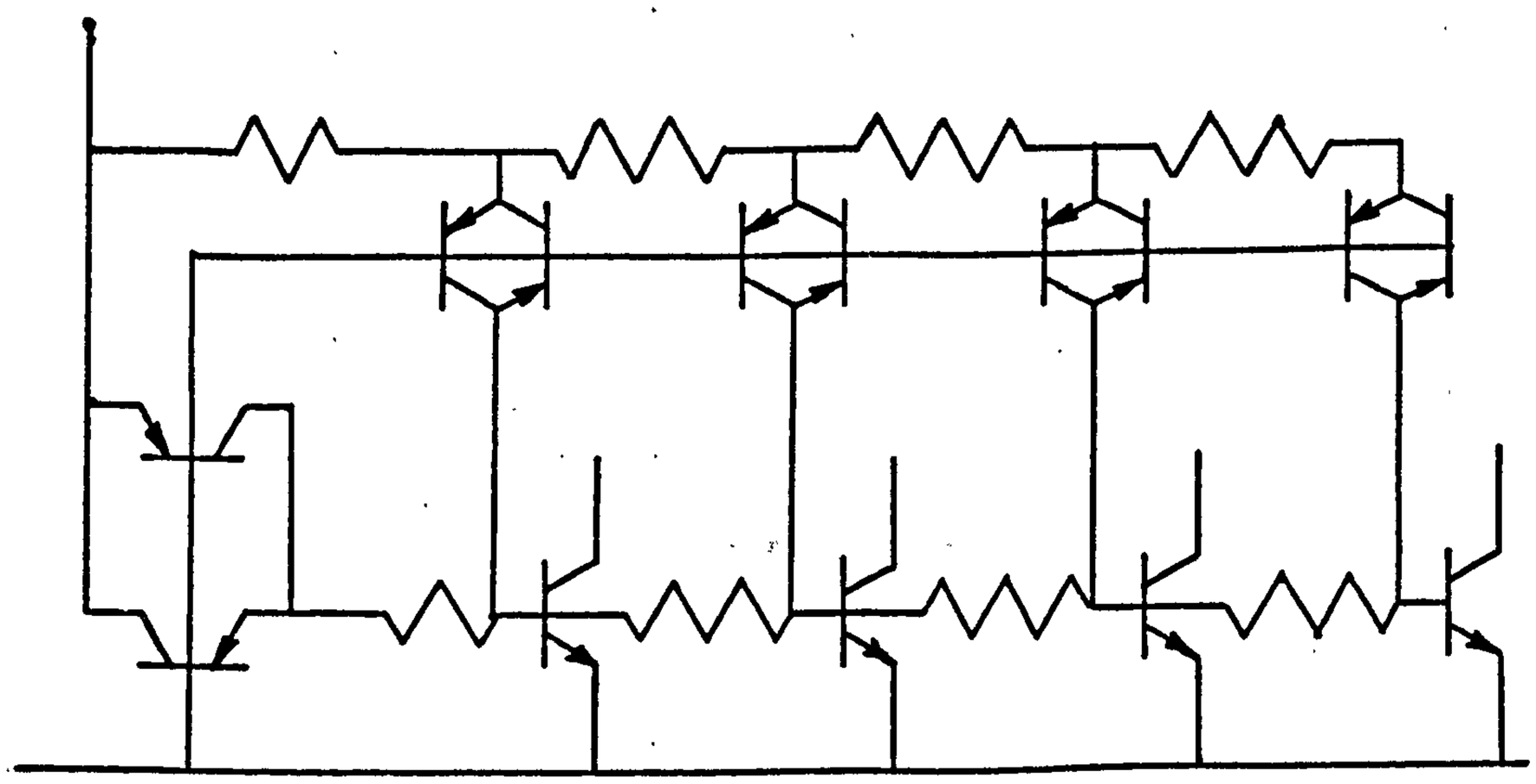


FIGURE 5.8.



Standard



Interdigitated

Equivalent circuit 4-collector I^2L gates.

FIGURE 5.9.

Injector current v gate delay. 4-collector Interdigitated gate (9-stage ring oscillator).

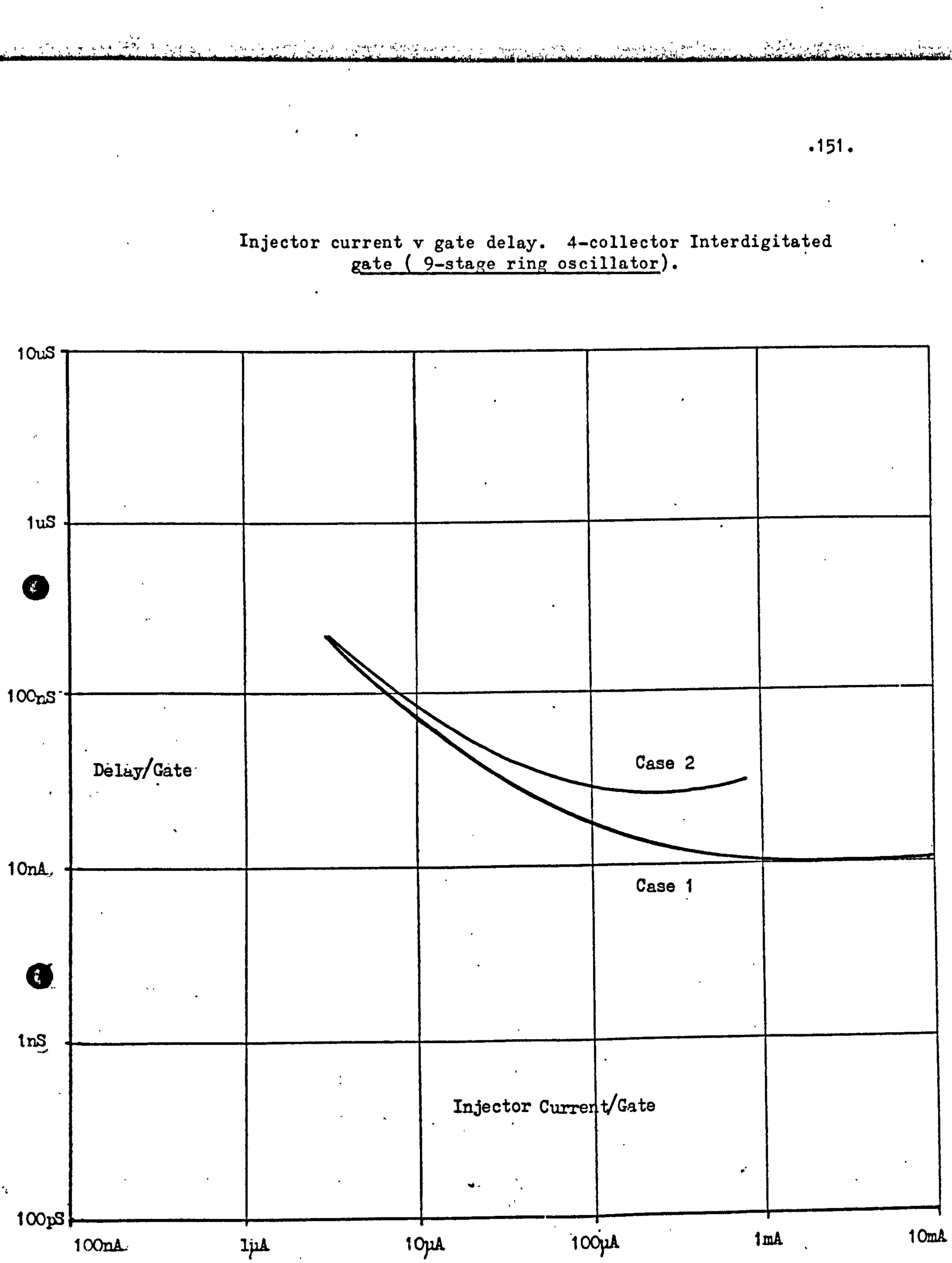


FIGURE 5.10

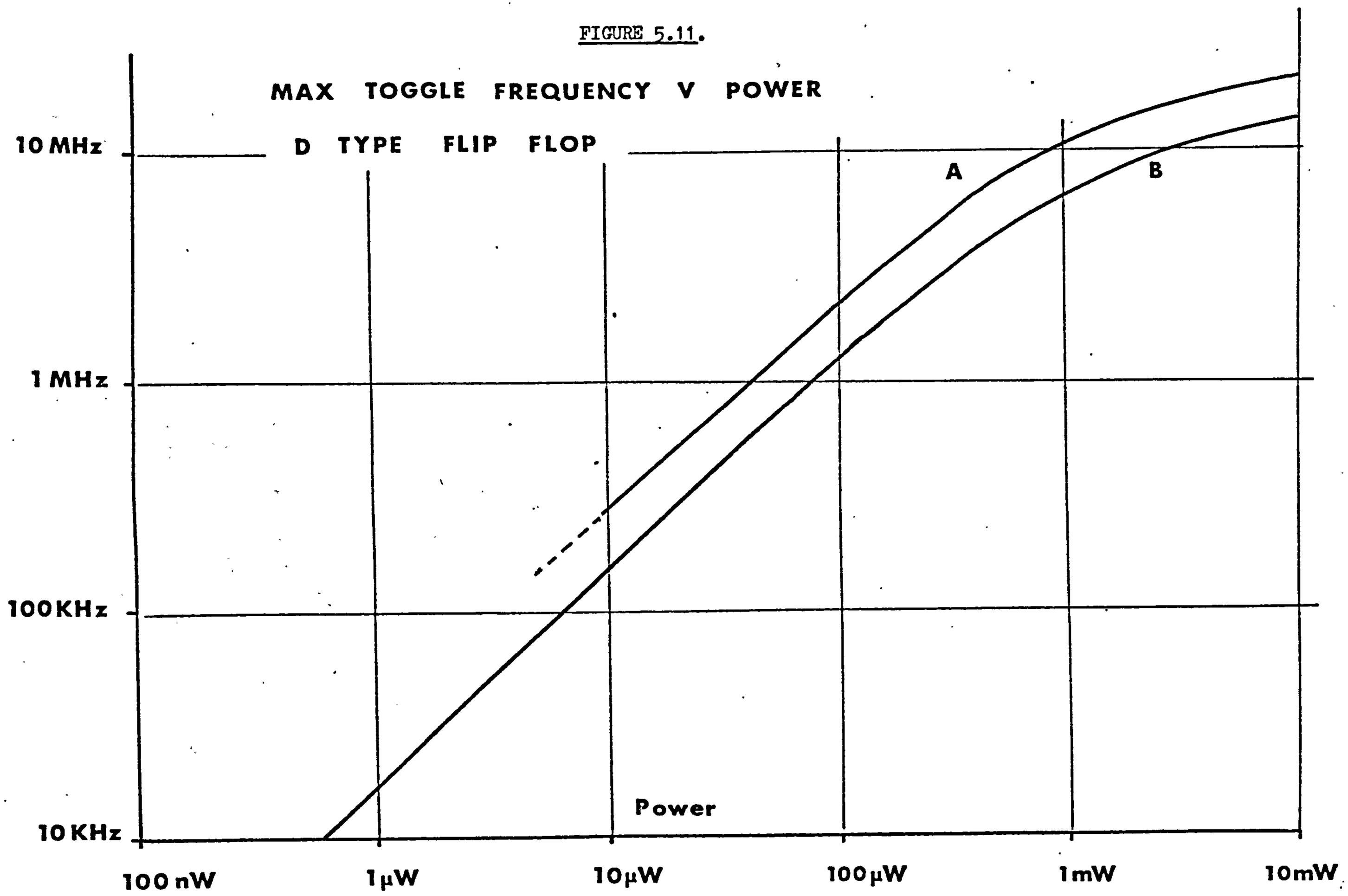
delay is also improved as a consequence of reduced charge storage in the epitaxy. The differential gate delay between the first and fourth collectors has been reduced by at least a factor of 2. However, the minimum power of operation has been degraded. This is because the lateral re-injection component of the upward npn base current has been increased by about a factor of 2. Thus the upward npn gain has been reduced. As β_u is a strong function of current, the current giving an upward gain large enough to sustain oscillation is also increased.

5.4. SPEED POWER CHARACTERISTICS OF D-TYPE FLIP-FLOP FABRICATED ON PROCESS III

Figure 1.8b Chapter 1 showed the logic diagram of an I^2L D-type flip-flop. Figures 5.11 a) and b) show the characteristics of D-type flip-flops connected as a divide-by-two function. ($\overline{Q}$ output connected to data input). This is the D-type toggle, and the output frequency is half the clock frequency. In the toggle configuration the maximum operating frequency is six gate delays, for a symmetrical clock input.

Case a) is a D-type fabricated using interdigitated injector and case b) is the standard gate configuration. This characteristic clearly shows the advantages of the interdigitated injector gate for high speed operation. The lower power delay product of the interdigitated gate is also evident as the interdigitated D-type operates at higher frequencies for a given power. The low power operation of the interdigitated D-type

FIGURE 5.11.


MAX TOGGLE FREQUENCY V POWER
D TYPE FLIP FLOP
10 MHz
1 MHz
100 KHz
10 KHz
A
B
Power
100 nW
1 µW
10 µW
100 µW
1 mW
10 mW

is inferior to that of the standard gate as a consequence of degraded low current βu as mentioned in the case of interdigitated ring oscillators. However, maximum speed of operation is increased from 13MHz to 20MHz.

The observed characteristics of the interdigitated injector D-type flip-flop and ring oscillators demonstrate the validity of this approach for the reduction of differential gate delays, and the improvement of maximum speed of operation.

5.5. PROCESS D EXPERIMENTAL RESULTS

5.5.1. D.C. Operation

Experimental observations of βu on Process D four collector I^2L gates produced the characteristic observed in Figure 5.12. This characteristic shows less evidence of debiasing than the Process III gate. This is because the base resistance is approximately 200 $\Omega/\square$ as against 500 $\Omega/\square$ for Process III.

5.5.2. Power Delay Characteristics of Ring Oscillators fabricated on Process D.

The Power Delay Characteristic of single and multi-collector ring oscillations fabricated on Plessey's Process D have been measured. These results, Figure 5-13, show a device with approximately an order of magnitude inferior minimum gate delay to Process III structures and a three-fold increase in power delay product. These experimental results are in agreement with the derived theoretical relationships of Chapter 4. The power delay product is proportional to junction area whilst minimum gate delay is proportional to epitaxy volume. The observed differences in parameters between

Measured βu v. I_B Characteristic Process D Four-Collector I^2L Gate

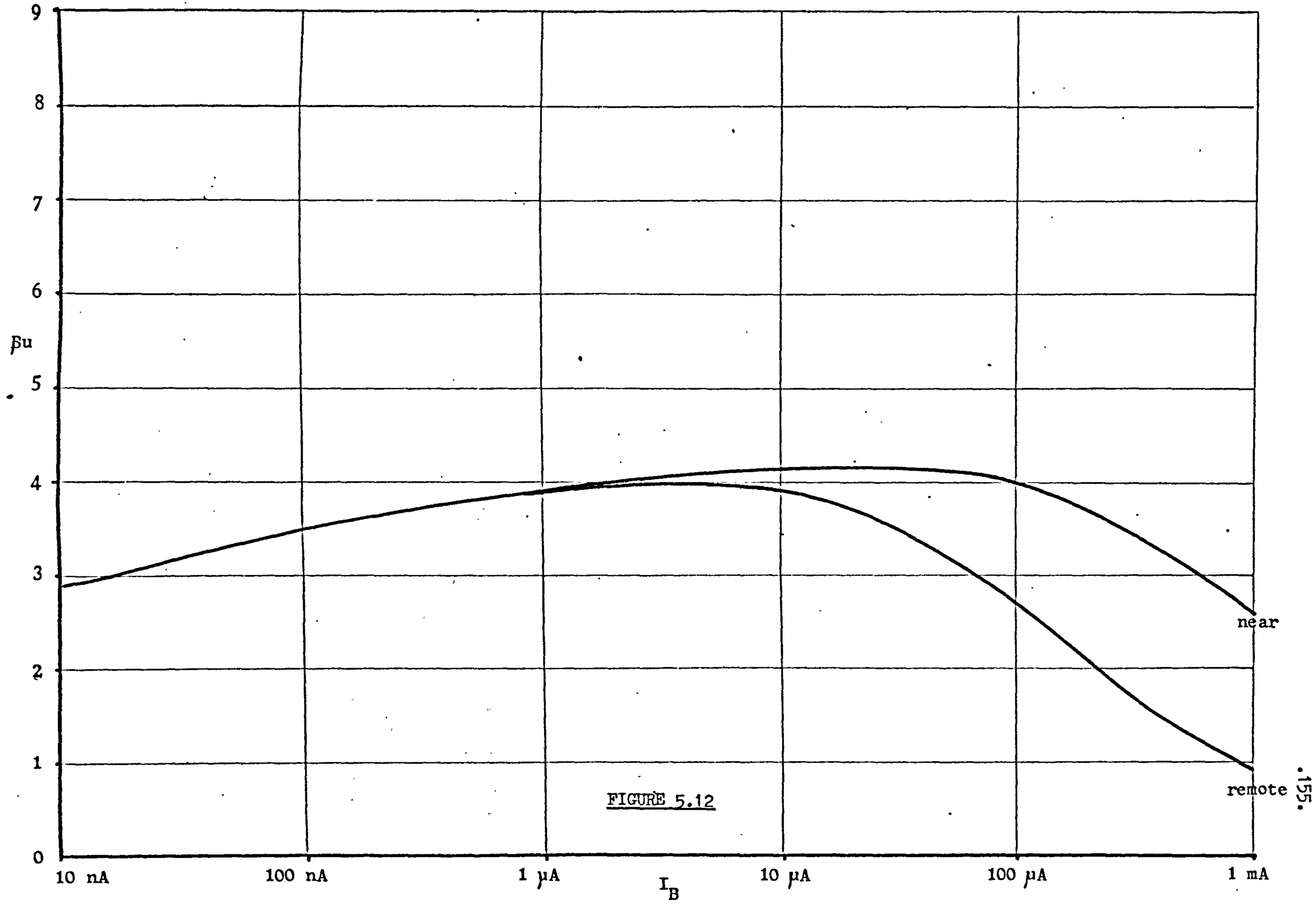
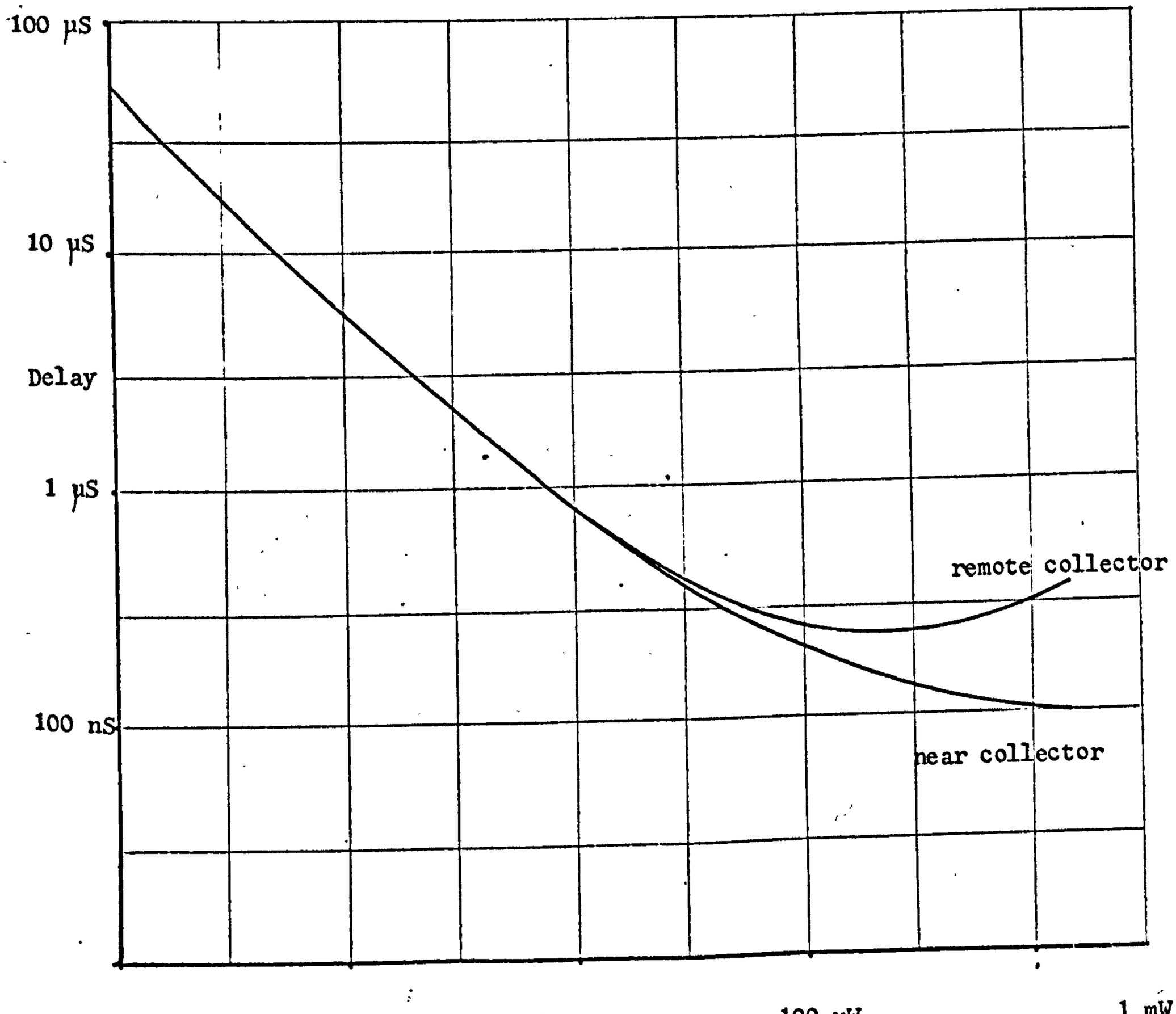


FIGURE 5.12

FIGURE 5.13.

Process D Four-Collector Gate

Power Delay Characteristic from Ring Oscillators



Process D and Process III I^2L verify the relationships, if correct dopings are included in the calculations.

The differential delay between the collector nearest and most remote from the injector is shown to be reduced as compared to Process III I^2L. This is a direct consequence of the reduced de-biasing on the D Process as evidenced from the D.C. gain characteristics.

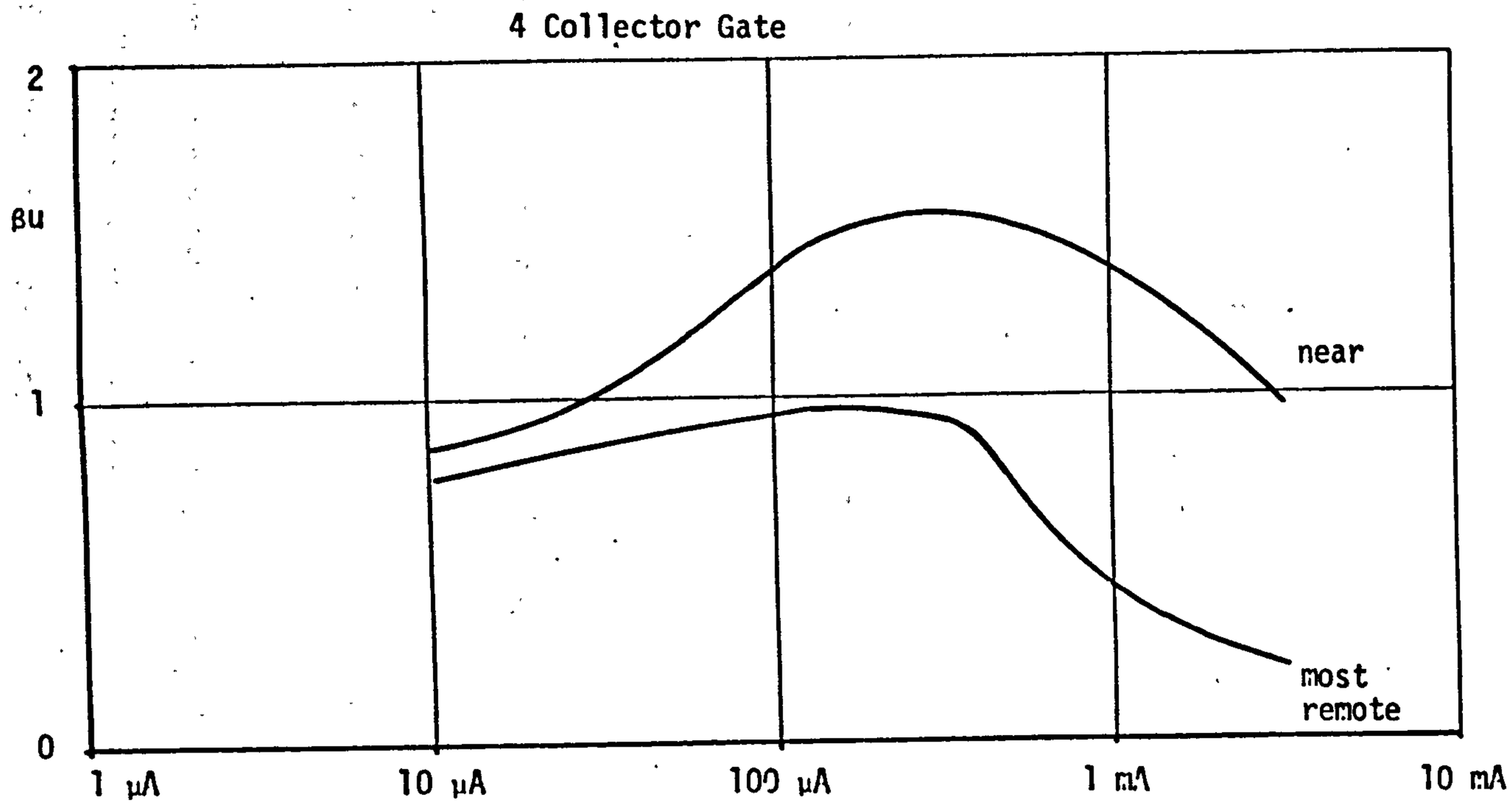
5.6 Process H Experimental Results.

5.6.1 D.C. Operation.

Calculations of upward gain β_u for likely process H gate structures indicated it was unlikely to be sufficient for I^2L operation. A number of process H batches of the test mask used to evaluate process D were produced. A typical experimental gain characteristic of the four collector gate is shown in Fig. 5.14. Maximum βu is of the order of 1.5, this agrees closely with the calculated value shown in Fig 3.23, and is too small for the operation of I^2L circuits. Alternative gate structures suitable for process H have been proposed (Appendix 2 Fig A2.2). However, these gates have yet to be fabricated.

FIGURE 5.14

EXPERIMENTAL βu v I_B CHARACTERISTIC HIGH VOLTAGE PROCESS



DISCUSSION

The previously developed I^2L theory has predicted that gain (βu) is dependent on processing and geometric factors, and on surface recombination rate, lateral re-injection and base collector area ratio. The experimental evidence supports these assertions, since both surface recombination and lateral reinjection have been shown to modify gain. From the presented βu data it is evident that if two collectors are used in parallel the effective gain is increased as the relationship between collector and base area predicts.

The dynamic behaviour of the I^2L gate is shown to be related to surface geometry in the manner predicted by theory. That is power delay product is proportional to junction capacitance, and minimum gate delay is proportional to gate fan out, the volume of low doped epitaxy, and the upward collector current available to change the charge stored in the device.

The differential delay between collectors on an I^2L gate is shown to be a consequence of D.C. debiasing, and that a more uniform distribution of base drive tends to reduce delay differences between collectors.

Process III I^2L has been subjected by the author to a comprehensive characterisation exercise. The results of this exercise are presented in Appendix 1 which detail measured values of Process III I^2L parameters.

CHAPTER 6

PARAMETRIC RELATIONSHIP AND PROCESS CONTROL IN I^2L

6.1. INTRODUCTION

The purpose of this chapter is to develop relationships between transistor parameters which will enable the rapid determination of I^2L gate parameters from downward transistor measurements. The relationships will also determine the compatibility between normal mode operation and I^2L performance. For example: are the gate delays required of a given I^2L circuit compatible with the voltage requirements of peripheral conventional circuits? Although these relationships have been introduced in chapters 3, 4 and 5 they are of such importance and significance that they justify being collected together. The specific treatments given are for Process III; however the approach with suitable modification are applicable to any process.

6.2. BREAKDOWN VOLTAGE ON PROCESS III

6.2.1. Radius of curvature effects and field intensification.

The breakdown voltage BV of a reverse biased one sided pn step junction in which the impact ionization process dominates is given by:

$$BV = \mathcal{E}_{crit} \frac{W}{2} \qquad 6.1.$$

where $\mathcal{E}_{crit}$ is the maximum allowable field and W is the width of the depletion region at this field. The maximum allowable field is the field at which carrier ionization occurs, and a small increase in field results in a rapid increase in current. The value of $\mathcal{E}_{crit}$ is dependent on electron and hole

ionization rates.

For an abrupt one sided junction of background doping N_B equation 6.1. becomes

$$BV = \frac{\epsilon_s \mathcal{E}_{crit}^2}{2q\ N_B} \qquad 6.2.$$

where ϵ_s = dielectric constant of semiconductor.

The simple introduction given above is not adequate to explain the observed experimental breakdown voltages on Process III. The real devices have graded junction, and most important, the junction perimeter has a radial diffusion front (radius equal to the junction depth). The corners of any diffusion window result in a diffusion front with a spherical surface.

The effect of junction curvature has been calculated (see ref. 42 page 121) and shown to result in a field intensification and a consequent lowering of breakdown voltage.

In general this effect is more important than the graded doping especially on Process III which with its shallow diffusions gives a really abrupt doping profile.

$$BV \simeq 60\left(\frac{E_g}{1.1}\right)^{3/2} \left(\frac{N_B}{10^{16}}\right)^{-3/4} \left\{\left[(n+1+\gamma)\,\gamma^n\right]^{1/(n+1)} - \gamma\right\} \qquad 6.3.$$

where E_g = Energy Gap of semiconductor

n = 1 and 2 for cylindrical and spherical junctions respectively

$\gamma = x_{j/W}$

x_j = diffusion junction depth

W = depletion width at breakdown of a plain junction background doping N_B

(after Sze ref. 42 page 121)

Putting typical values for Process III into equation 6.3. results in:

$$BV \simeq 25 \quad \text{to} \quad 35V$$

Collector base breakdown voltages greater than these values are limited by junction curvature effects

6.2.2. Reach Through

Most epitaxial silicon devices include a heavily doped buried layer. If the distance between the junction and the NN^+ interface is smaller (Figure 6.1) than the depletion width at breakdown of a normal $P^+ N$ diode without the buried layer, additional potential builds up across the low doped N epitaxial region. Maximum field is attained earlier than the simple case without N^+. Assuming

$$N^+ \gg N \text{ and } W_E \gg W_{crit}$$

$$BV = -\int_0 \mathcal{E}\, dx$$

$$= -\left(\mathcal{E}_{xc} W_E + (\mathcal{E}_{max} - \mathcal{E}_{xc}) \frac{W_E}{2}\right)$$

$$= -\left(\mathcal{E}_{xc} \frac{W_E}{2} + \mathcal{E}_{max} \frac{W_E}{2}\right)$$

$$\text{now} \quad \mathcal{E}_{xc} = \mathcal{E}_{crit} - q \frac{N_D}{\epsilon_s} W_E \qquad 6.4.$$

from Poissons equation.

Where $\mathcal{E}_{xc}$ is the field at $N N^+$ interface and $\mathcal{E}_{crit}$ is the value of $\mathcal{E}_{max}$ at breakdown.

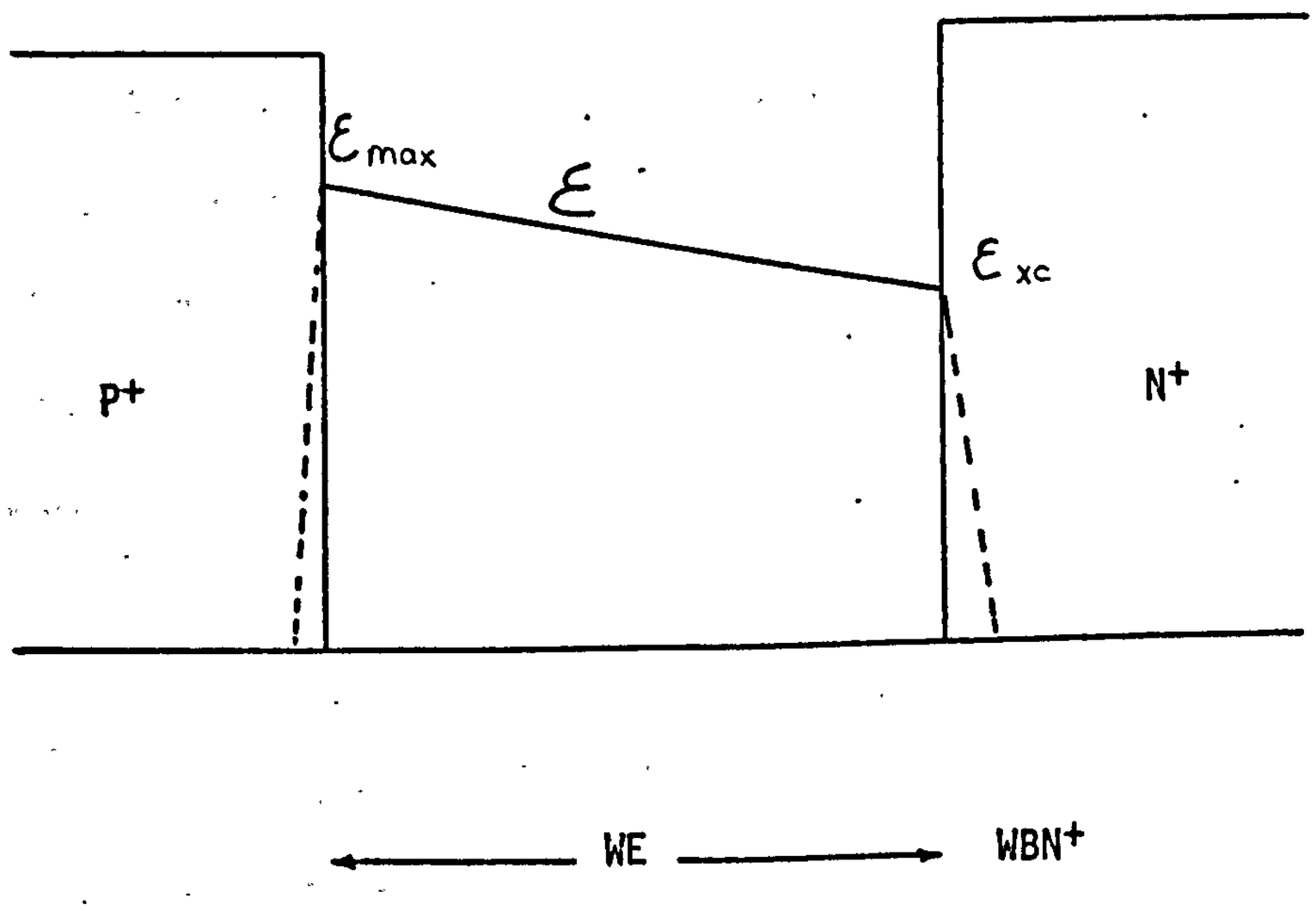


FIGURE 6.1

Electric field distribution in reverse biased P^+NN^+ diode

$$BV = \mathcal{E}_{crit} W_E - q \frac{N_D}{2\epsilon_s} W_E^2 \qquad 6.4.a.$$

As a consequence of equation 6.3. values of BV_{CBO} below 25V are controlled by the doping and thickness of the epitaxy. In Process III the P^+ resistor diffusion used to contact base has a junction depth of 0.8 μm in comparison with 0.4 μm for the base and 0.6 μm for the intrinsic run-on base. This difference has to be taken into account when calculating BV_{CEO} (see next section)

6.2.3. Collector emitter Breakdown BV_{CEO}

The collector emitter breakdown voltage of an open circuited base transistor can be controlled by either the punch through or avalanche multiplication. For the latter case breakdown BV_{CEO} can be calculat ed as follows:

The collector current is the sum of the collector-base leakage plus the collected current, thus:

$$I_c = I_{CBO} + \alpha I_E$$

Now $I_c = I_E = I_{CEO}$ and therefore

$$I_{CEO} = I_{CBO} + \alpha I_{CEO}$$

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha M}$$

The factor M is the collector multiplication factor due to the effects of avalanche breakdown (. 38)

$$M = \frac{1}{1-(BV_{CEO}/BV_{CBO})^n} \qquad 6.5.$$

where BV_{CBO} is the true breakdown of that part of the collector

(no page 164)

junction at the intrinsic base of the transistor. At BV_{CBO}, I_{CEO} becomes infinity. For this to happen

$$\alpha M = 1$$

$$M = \frac{1}{\alpha}$$

Solving for BV_{CEO} in 6.5.

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{(1-\alpha)}} \simeq \frac{BV_{CBO}}{\sqrt[n]{\beta_d}} \qquad 6.6.$$

Where BV_{CBO} in this case is defined by reach through to buried N^+ from the run-on base. And n is a factor approximately equal to 4 for npn transistors on Process III. (38, p.232).

In the alloy type transistor the collector emitter breakdown voltage can be punch through limited. This is when the expanding collector base depletion layer touches the emitter base depletion region. In the alloy transistor the collector base junction is approximately a one sided step junction with the base the lowly doped region. Then the punch through voltage V_{pt} is

$$V_{pt} = q\frac{N W_B^2}{2\epsilon_S} \text{ (from simple diode theory)}$$

and $BV_{CEO} = V_{pt} + \phi_B$

ϕ_B is built in voltage of the emitter base junction

In an epitaxial transistor a similar phenomena can occur. as the depletion region in the epitaxy is pinned by the Buried N^+ region. Once the lower edge of the depletion region reaches

the buried N^+ the depletion edge in the base itself will move towards the emitter. In this case it is possible for the depletion region in the base to punch through to the emitter before avalanche occurs.

For the punch through condition we must sum the voltages - across the base and epitaxial parts of the depletion region.

In the base depletion region the voltage necessary for punch through is (assuming abrupt doping profiles for simplicity)

$$V_{base} = q \frac{N_A W_B^2}{2 \epsilon_s} \qquad 6.7$$

Using the arguments which were used to develop equation 6.4.a (Reach through), but now saying that the peak field is less than $\mathcal{E}_{crit}$ then the voltage developed across the epitaxy V_E is

$$V_E = \mathcal{E} W_E - q \frac{N_D W_E^2}{2 \epsilon_s} \qquad 6.8.$$

where $\mathcal{E}$ is peak field.

But using equation 6.1. $\mathcal{E} = \frac{2 V_{base}}{W_B} = q \frac{N_A W_B}{\epsilon_s}$

$$\therefore V_E = q \frac{N_A W_B W_E}{\epsilon_s} - q \frac{N_D W_E^2}{2 \epsilon_s} \qquad 6.9.$$

The punch through voltage is then $V_{base} + V_E$

$$V_{pt} = q \frac{N_A W_B^2}{2 \epsilon_s} + q \frac{N_A W_B}{\epsilon_s} W_E - q \frac{N_D W_E^2}{2 \epsilon_s} \qquad 6.10$$

For the base of a 'real' transistor the simple approximation

$$N_A W_B = \int_0^{W_B} N_A(x)dx$$

can be made. Then

$$V_{pt} = \frac{q}{2\epsilon_s} \int N_A \, dx \, W_B + q \int \frac{N_A \, dx}{\epsilon_s} \, W_E - q \frac{N_D W_E^2}{2\epsilon_s} \qquad 6.11$$

Equations 6.4q, 6.6 and 6.11 therefore define all the primary breakdown voltage parameters for the downward mode conventional npn device. These downward mode parameters are all shown to be dependent on epitaxial parameters, i.e. base buried N^+ clearance and epitaxial doping. In chapters 3 and 4 it was shown that these parameters have a dominant effect on the control of I^2L upward mode operation, both β_u and minimum date delay.

In chapter 3 the fact that upward and downward gain are related through a common dependence on integrated base doping was introduced. This fact enables the development of a comprehensive set of design criteria for I^2L, which show the relationship between desired downward transistor characteristics and obtainable compatible I^2L characteristics.

Relationship between β_u and β_d

It is found experimentally on Process III that gain variations between batches and wafers is due mainly to variations in integrated base doping. This is illustrated in

PROCESS III DOWNWARD TRANSISTOR COMPARISON
HIGH, LOW βu DEVICES

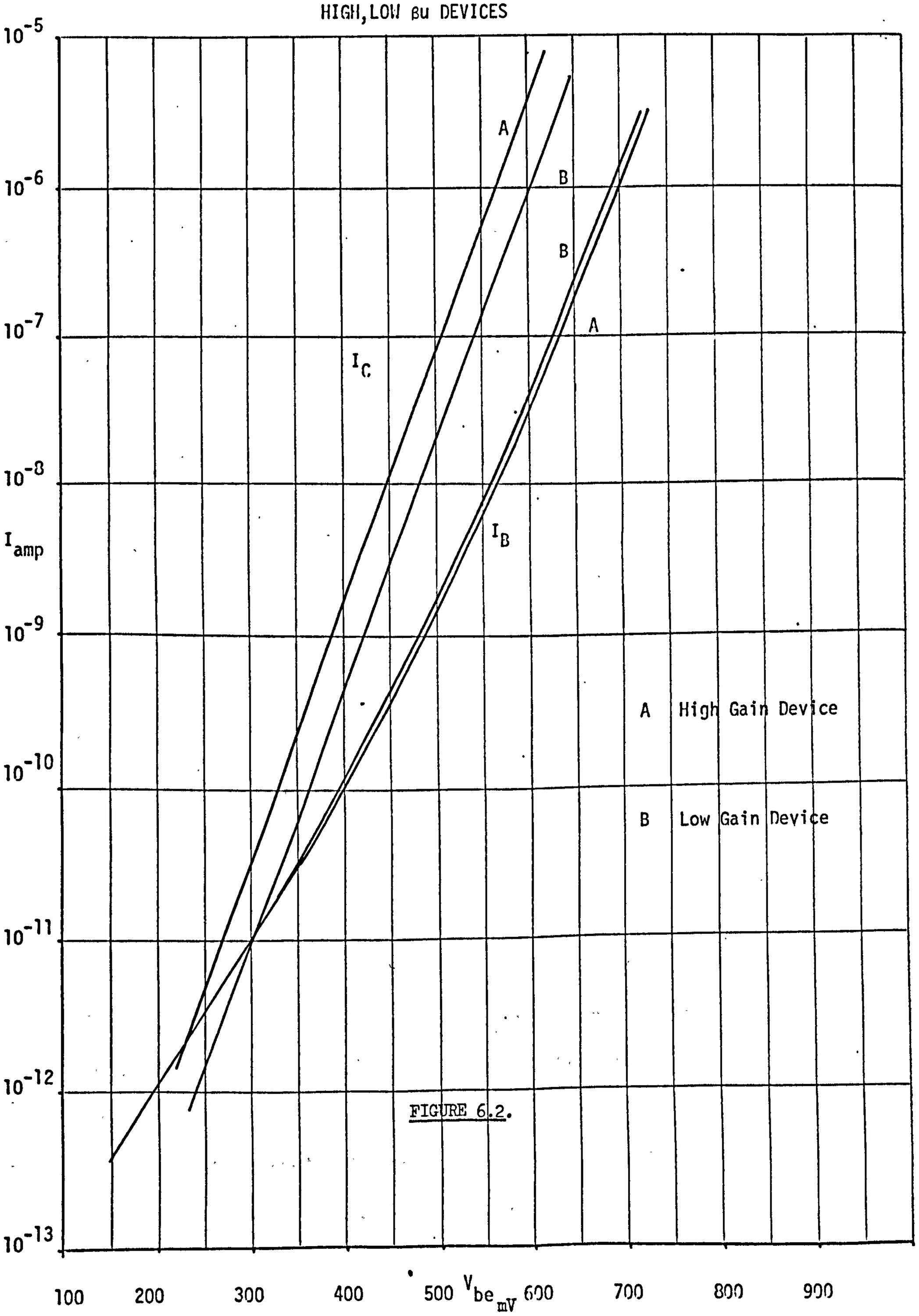


FIGURE 6.2.

Fig. 6.2 which shows V_{be} I_c I_b characteristics for two Process III npn transistors. The characteristics were obtained by measurement at the same time, but the devices were manufactured one year apart. These characteristics clearly show base currents to be virtually the same, whilst collector currents are very different. Thus the difference in β_d of these two devices is because the collector current of the devices is markedly different at a given V_{be} whilst base current is not.

Now in the medium injection regime

$$\beta_d = \frac{I_c}{I_b}$$

$$\beta_d \simeq \frac{q\, n_i^2\, D_n}{\int N_A dx} \exp qV/KT \cdot \frac{1}{I_{BO} \exp q\, V/KT}$$

$$= \frac{q\, n_i^2\, D_n}{\int N_A\, dx} \cdot \frac{1}{I_{B0}}$$

As seen demonstrated in Figure 6.2

$$\therefore \quad \beta d = \frac{D_n}{\int N_A dx} \cdot \frac{1}{K} \qquad 6.12$$

$$\text{Now } \beta u = \frac{q\, n_i^2\, D_n}{\int N_A dx} \text{ exq } (qV/KT) \cdot \frac{1}{I_B \exp qV/KT}$$

$\frac{D_n}{\int N_A dx}$ is the Gummel number (43)

In chapter 3 section 3.4. it was shown that the collector current of the I^2L gate before the onset of high level injection is controlled by this parameter. Thus Gummel number controls collector current of the upward and downward transistor if Dn is considered doping independent. The doping integral

across the intrinsic base $\frac{1}{\int N_A dx}$ is identical for both the upward and downward mode devices, with the limitations that depletion layers are not modified for upward downward conversion and the device is not in high level injection.

Further if the average minority carrier diffusion coefficient in the base D_n is considered independent of mode of operation equation 6.12 can be transposed as follows:

$$\frac{D_n}{\int N_A dx} = \beta dK \qquad 6.13$$

Thus downward gain βd can be used to specify Gummel number and βu is thus dependent on βd, as is shown in Figure 3.18. NOTE also that $\int N_A dx$ appears in equation 6.11, and 6.13 can be substituted into this relationship.

Figure 6.3. shows the theoretical relationship between β_d BV_{CEO} and BV_{CBO} with the onset of punch through defined by the solution of equation 6.11 with the substitution of the gain dependency of integrated base doping as defined by equation 6.13.

In chapter 4 expressions for the intrinsic gate delay of the I^2L gate are derived. The value of intrinsic delay is shown to be heavily dependent on the common emitter angular cut-off Frequency ω_T.

$$\omega_T = \frac{dI_c}{dQ_T}$$

$$\simeq \frac{I_c}{Q_T}$$

$$= \frac{A_C}{A_B} \frac{D_n \; N_{D_{EPI}}}{\int N_A dx \; W_E} \qquad 4.3.$$

Relationship between BV_{CEO} BV_{CBO} β_d

and Base Buried N+ Clearance

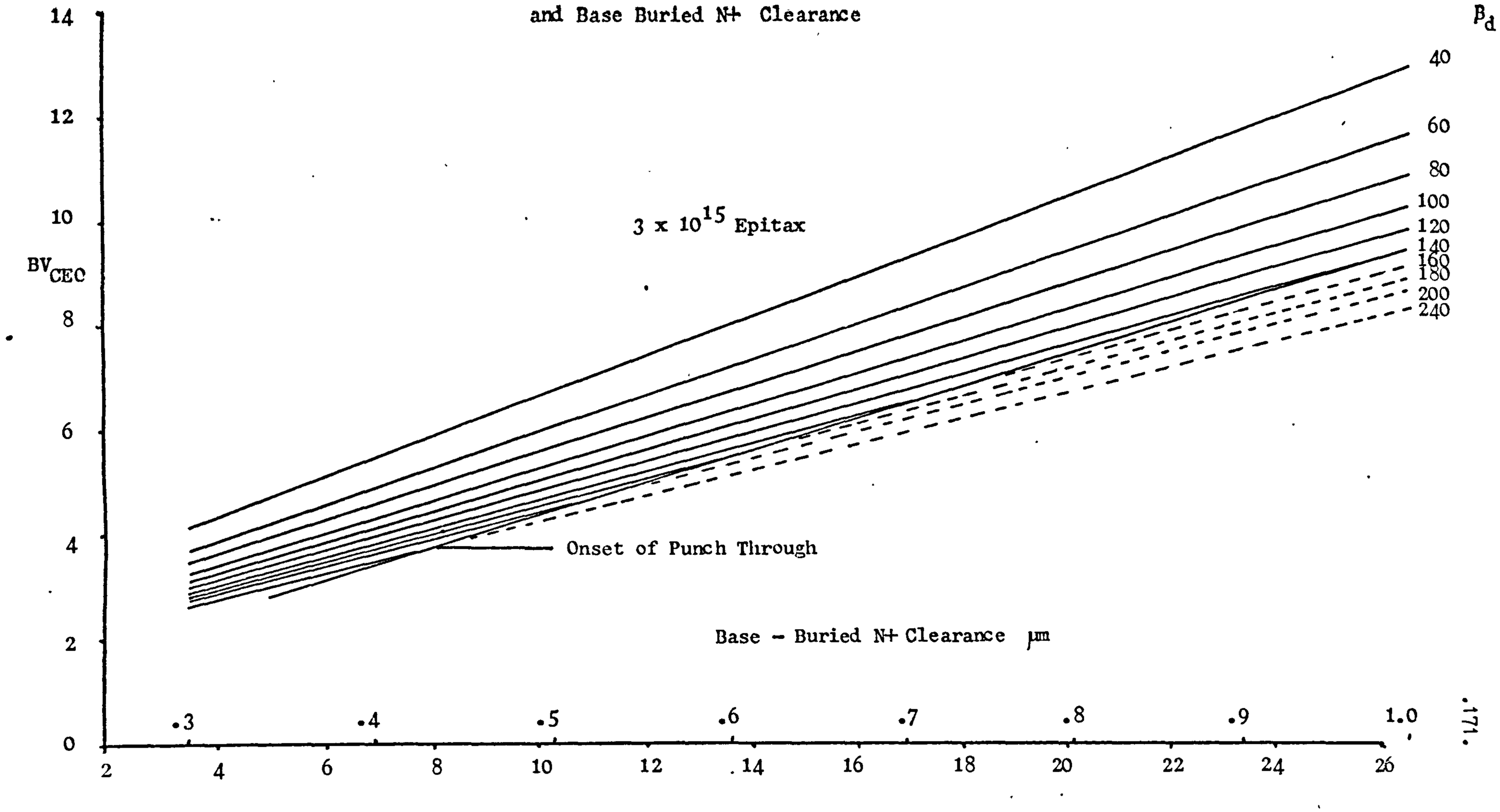


FIGURE 6.3.

NOTE a more rigorous deriviation gives

$$\omega_T \simeq \frac{n_i^2 D_n \{\exp (qV/KT)\}.A_C}{\{\int N_A \, dx + p_o (W_{B/2} + W_{EPI})\}\{PoA_B W_{EPI}\}}$$

from equation 4.3(b) and 4.3(c) where p_o is as defined in equation 3.1.

Equation 6.13 can be substituted into 4.3. or into the more rigorous derivations as developed in chapter 4. Thus ω_T of the I^2L device is related to the conventional downward mode gain βd.

Hence, from a knowledge of βd and BV_{CBO} two major parameters of importance to I^2L (βu and t_{di}) operation can be estimated (Figure4.8). These relationships have been found to be valid for process III. (See tables 5.1 and 6.1) Confirmation has also been obtained using Process D as shown in table 6.2. Initial experiments on an ion-implanted shallow junction process at Plessey Caswell (process WV), which is similar in final structure to process III also tend to support the developed relationships.

DISCUSSION

In an extension of earlier theoretical treatments the relationship between I^2L and conventional devices has been further developed. In particular, the major I^2L parameter βu and t_{di} are related to conventional device parameters (βd and Breakdown voltages). It is shown that the interdependance of the parameters results in device constraints if conventional transistors and I^2L gates are to be included on the same chip. Graphical representaions are given with which these constraints are easily estimated, and

Table 6.1

βd	BV_{cbo}	t_{di} measured	t_{di} calc.
50	10	60ns	54ns
80	6	21ns	22ns
100	7	16ns	17ns
120	15	25ns	23ns
180	8	11ns	10ns
250	10	10ns	9ns

Process III

Experimental values of βd BV_{cbo} and minimum gate delay t_{di} compared to predictions from described theory.

βd	BV_{cbo}	BV_{ceo}	βumeas	βucal	t_{di} meas	t_{di} calc
70	64	23	1.4	1.2	240ns	200ns
150	62	20	2.3	2.4	104ns	118ns
200	59	17	3.8	3.7	81ns	84ns

Table 6.2

Process D

Experimental values of βd, $BV_{cb'o}$ β_u and minimum gate delay t_{di} compared with predictions from described theory.

processing can be easily toleranced.

CHAPTER 7

YIELD

7.1. INTRODUCTION

The first part of this work has been devoted to the development of a Physical understanding of the operation of the I^2L gate. However, a major objective in the use of I^2L is the production of LSI logic functions at commercial yields. This chapter is devoted to a description of the yield limiting phenomena which have been encountered in the manufacture of I^2L functions on Plessey's Bipolar Process III. The yield phenomena discussed here are those which result in catastrophic failure; parametric failure due to slight variations in the process is not discussed. The salient characterisation data for the Process is given in Appendix 1.

The catastrophic failure mechanisms discussed fall into two main categories, viz;

1) mechanical failures associated with mask making and photoengraving etc.
2) phenomena which result in an incorrect device structure; these effects include metallisation contact pitting, dopant penetration of masking oxides and collector emitter leakage, described as collector emitter piping.

The major failure mechanism encountered was without question the collector emitter piping. For this reason the work relating to the other failure mechanisms will be described first and the

remainder of the chapter will be devoted to the description of collector emitter piping and associated phenomena. The chapter will therefore be partitioned into Processing Phenomena and Collector-Emitter piping sections. "Piping" is a leakage path between the collector and emitter across the intrinsic base of the transistor. The pipe region has the properties of an n-type material in the devices investigated and piping is not associated with poor collector base or base emitter junctions.

7.2. PROCESSING PHENOMENA

7.2.1. Base Regrown Oxide

The initial I^2L development on Process III used a slight modification to the standard recut emitter variant of the Process (see Appendix 1). This process variant was little used for conventional circuits as the alternative bare emitter structures offer significant performance advantages for such techniques as emitter coupled logic. The recut emitter variant of Process III uses a 1000Å thermal regrown base oxide, whilst the bare variants have this oxide plus a 2000Å deposited oxide, making 3000Å total base oxide.

During the emitter phosphorus diffusion (shallow N^+) the upper part of the base oxide is converted to phosphorous glaze and the phosphorus diffuses into the base oxide in front of the phosphorous glaze. For a Process III shallow N^+ heat cycle it is possible for the phosphorus to penetrate 900Å of base oxide. If the base oxide is 900Å or less in thickness

the phosphorus penetrates to the base surface, forming an n-type "skin" across the surface of the device resulting in I^2L circuits with collector-collector leakage.

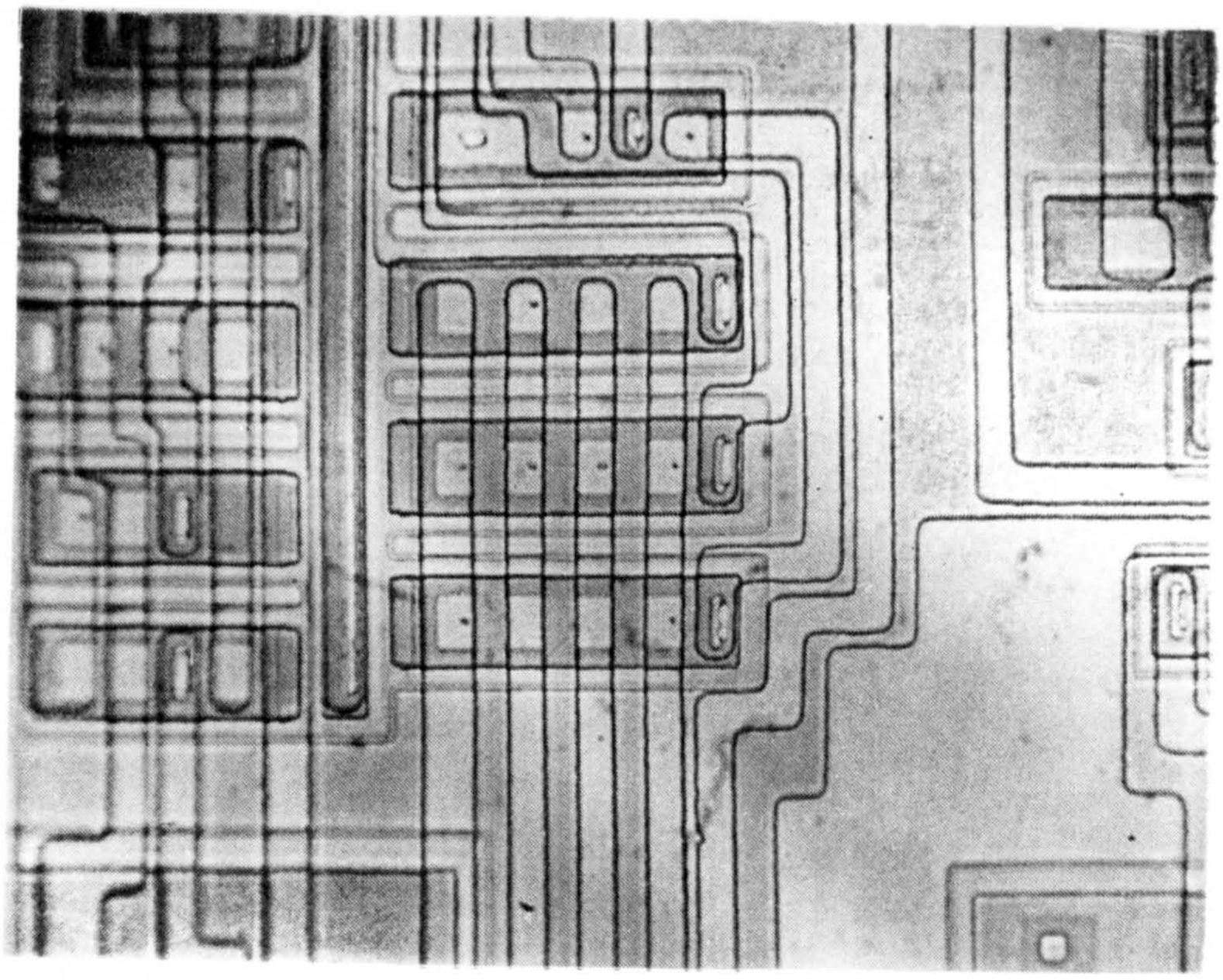
Although it does not happen often, two batches were found to suffer from phosphorus penetration of the base oxide. As a result of this the base drive-in schedule was modified to grow a 1200Å oxide. Since this modification this failure mechanism has not been observed. With the deposited oxide on the bare emitter Process III variants this is obviously unimportant.

7.2.2. Photo-engraving

A number of problems have been encountered with the photo-engraving of I^2L circuits. The first difficulty discovered was the photoengraving of the 6 x 4 micron shallow N^+ (I^2L collector) contacts. Figure 7.1. shows photographs of similar areas of adjacent chips from an I^2L wafer. The metallisation has been removed and it is fairly easy to see that some contact windows have not opened during contact etch. The problem was associated with two factors; the correct printing and developing of the photoresist (including exposure time) and little safety margin at contact etch. A small 'over etch' was added to the contact etch time: these procedures with improved inspection have eliminated the problem.

The next problem associated with photoengraving was finally traced to mask quality: Figure 7.2. shows an area of an I^2L circuit in which the base of a gate passes between a split

(a)



(b)

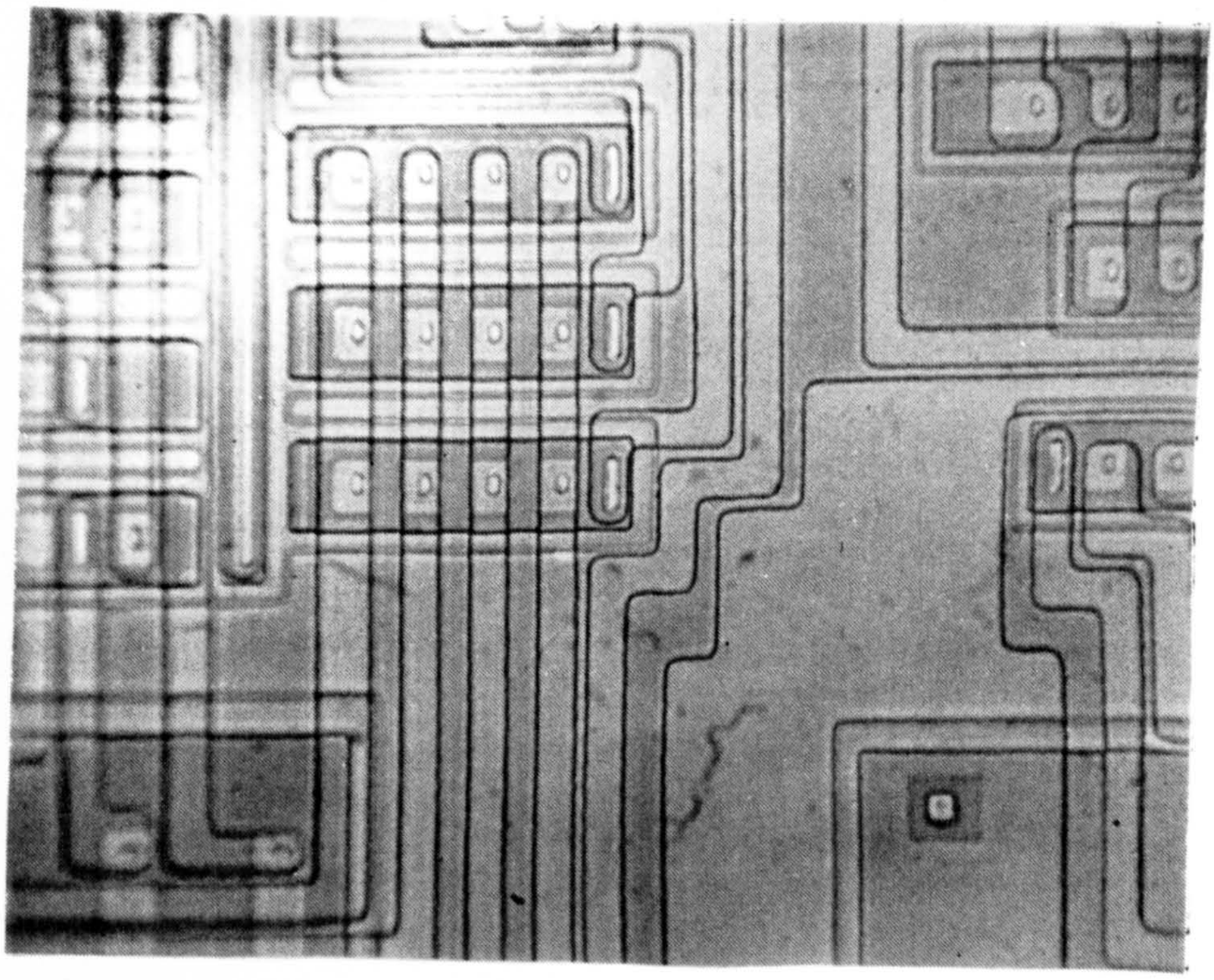


FIGURE 7.1 ADJACENT CHIPS

(a) Failure of 6 x 4 μm contacts to print and etch

(b) 6 x 4 μm contacts printed and etched

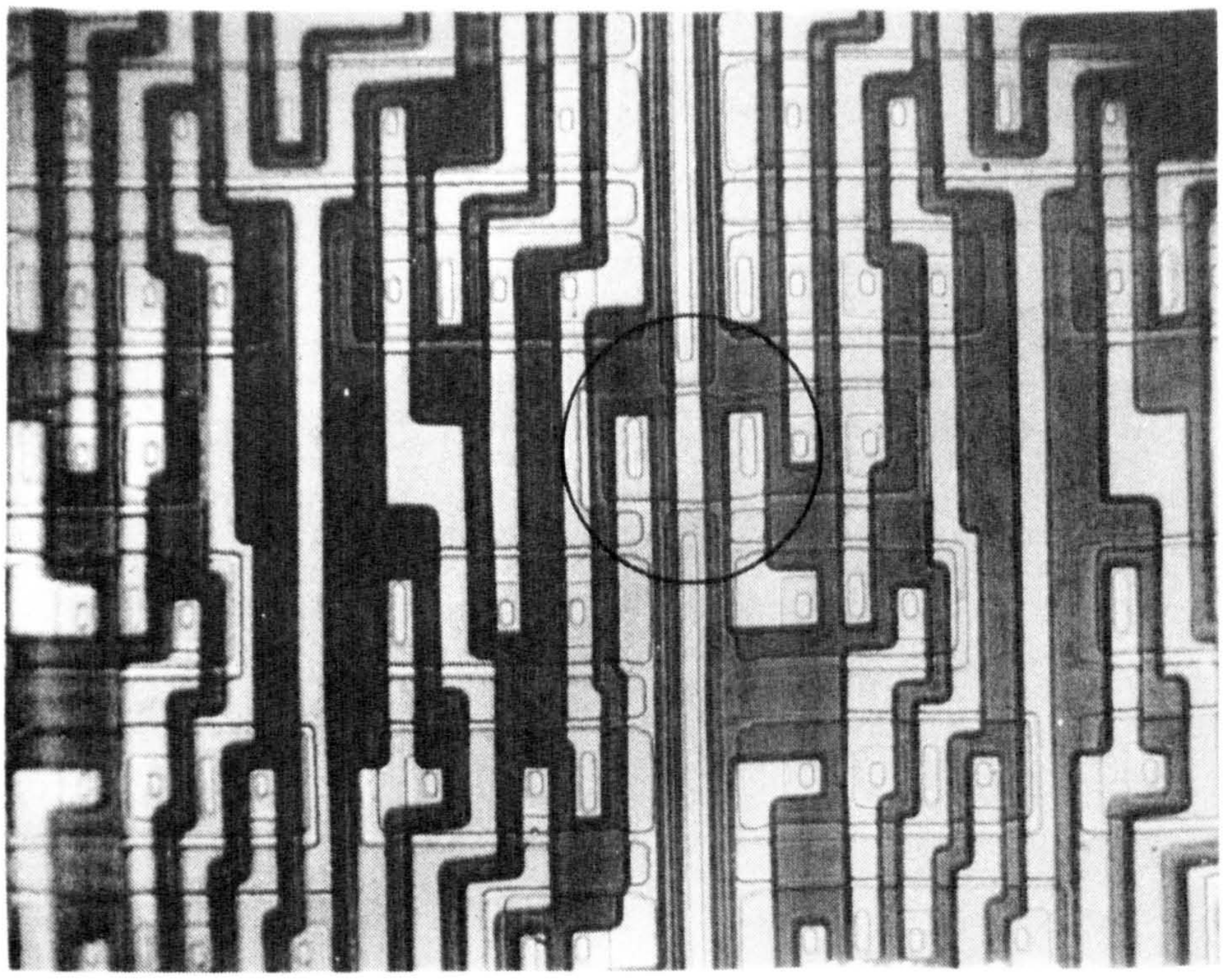


FIGURE 7.2.

Failed region is that within circ led area note clearance between injector and base of gate used to "cross-over" the injector.

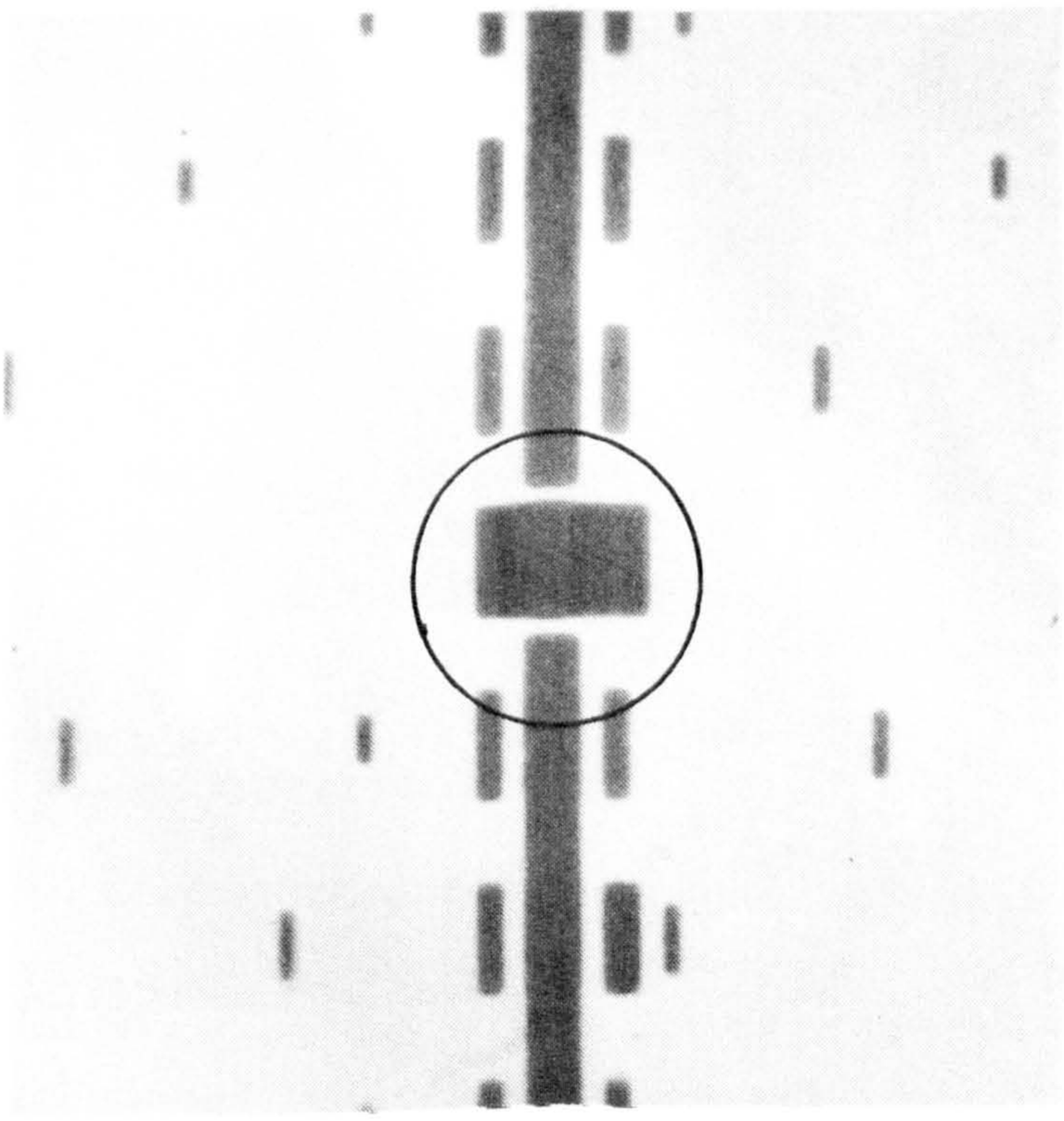


FIGURE 7.3(a)
CHROME MASK USED TO FABRICATE
DEVICE IN FIG.7.2

(Cut 'n' Strip Mask)

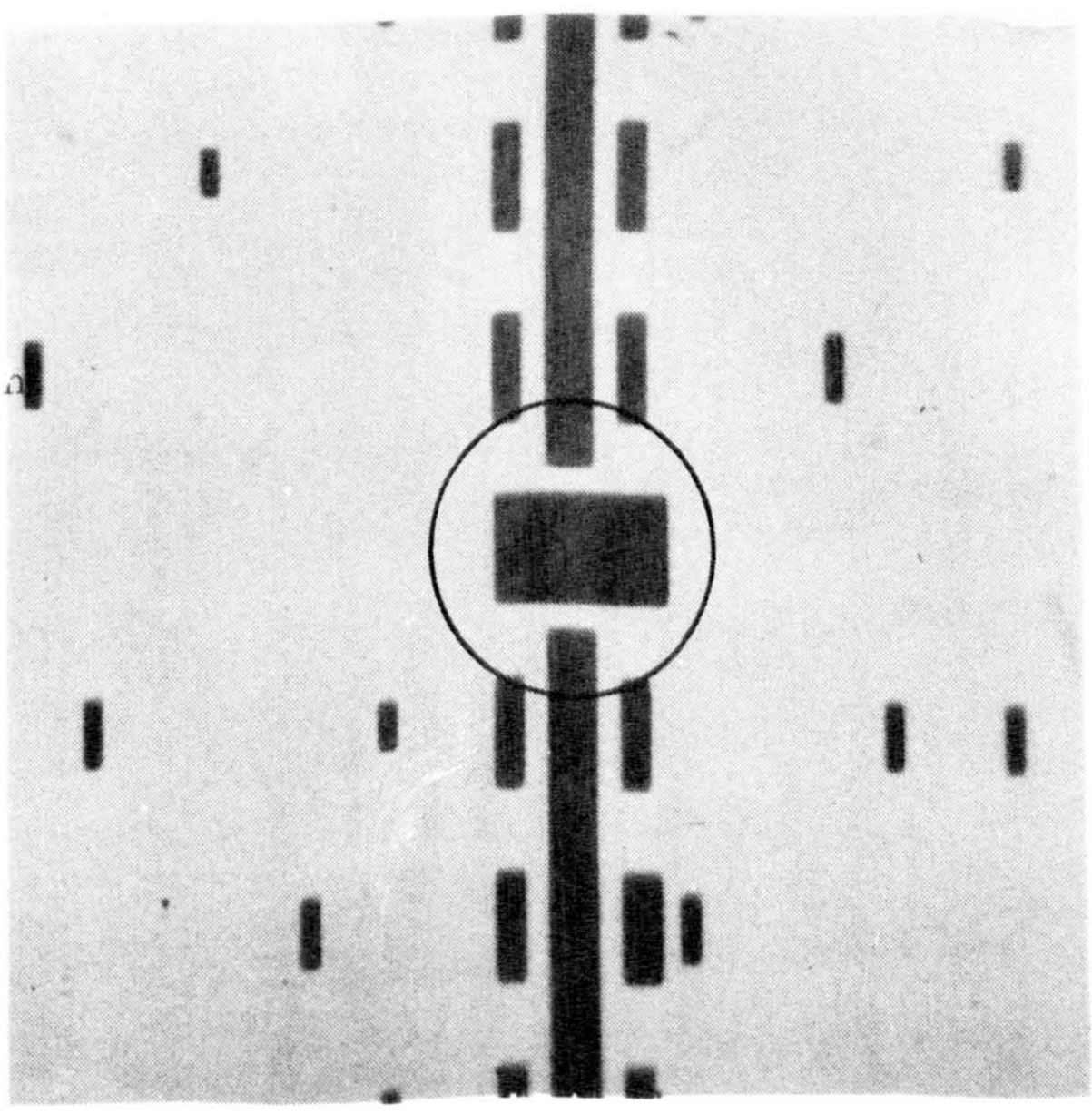


FIGURE 7.3(b)
CHROME MASK MANUFACTURED USING
DAVID MANN PATTERN GENERATOR

Dark areas are chrome areas on mask, these areas define windows in photoresist through which the oxide is etched. This is the P^+ mask; the long strips in the centre are injectors and the adjacent rectangles define the "bases" of the gates where they face the injector.

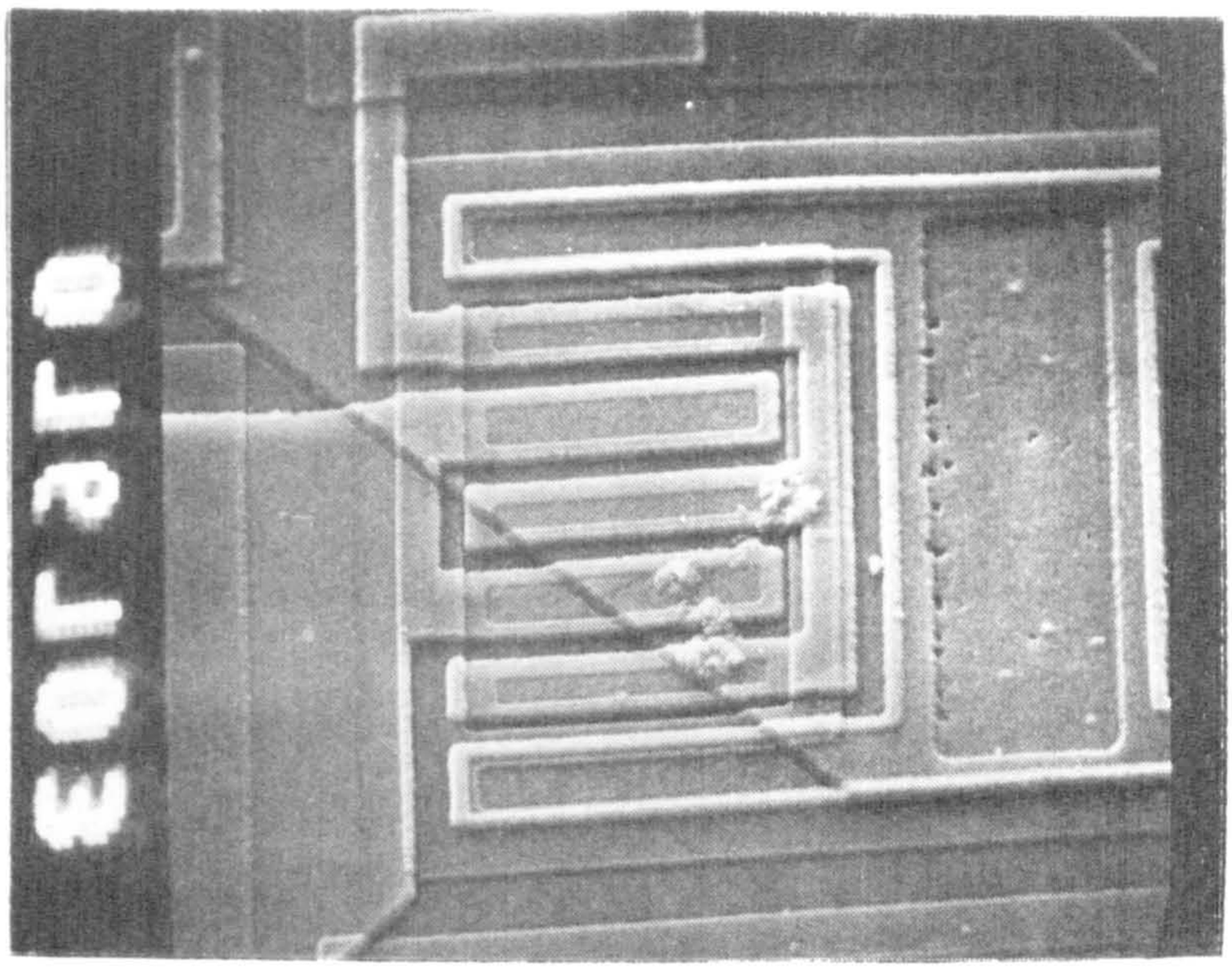
injector. The gate received its base current by injection from the two injector ends. The design clearance between the injector and gate is 4 μm; in this case this distance is less than 2 μm resulting in gate injector shorting. This effect was caused by defective mask making. Figure 7.3(a) shows the mask used to fabricate the device. This mask was manufactured using a convention artwork rubylith master (see ref.1 for details of mask making technology). The master, however, was generated from a computer graphics system. The computer graphics system produces a magnetic tape with the information necessary to drive an automatic cutting rather than a manual cut-and-strip table. Figure 7.3(b) shows the same region on another mask produced from the same magnetic tape. In comparison with Figure 7.3(a) this mask shows a clear improvement in dimensional accuracy. The mask for Fig.7.3(b) was manufactured using a David Mann pattern generator. In this system the mask pattern is obtained by exposing small portions of the circuit at a time onto an emulsion covered optical flat. This emulsion is approximately ten times the final size. The rubylith system which reduces 200 to 500 times from the original artwork suffers from optical interference/diffraction problems at line edges during the photo reduction process to final size. This results in the loss of dimensional accuracy observed in Figure 7.3(a). The problem only appears when adjacent windows are closely spaced and of the order 4 μm or less apart.

7.2.3. Metallisation

Process III is a shallow diffused process using ⟨100⟩ orientation silicon. This combination places a number of limitations on the metallisation technology. If pure aluminium is used during sinter (necessary to produce a low contact resistance), silicon diffuses into the aluminium in the contact regions leaving a void in the silicon (ref. 2). This void or 'pit' can be several microns deep. The aluminium also diffuses into the pit. On Process III with 0·4 um emitter (shallow N^+) junction depths, this results in an emitter-base short-circuit (Figure 7.4). The common solutions to this problem are either to include silicon in the aluminium deposition in sufficient concentration to prevent further diffusion from the silicon in the contact (i.e. pre-saturate to the solubility limit of the sinter temperature) or to interpose a barrier between the silicon and aluminium. This barrier layer prevents the aluminium and silicon coming into intimate contact. On Process III the barrier layer solution has been adopted and titanium is the material used. Process III uses 3000Å of titanium and 6000Å of aluminium. The titanium has other desirable properties such as excellent adhesion and increasing the metallisations resistance to electro-migration.

However, this system does have a number of problems. First the titanium thickness must be above a certain minimum as aluminium titanium solid state inter-diffusion occurs during

(a)
X490



(b)
X3000

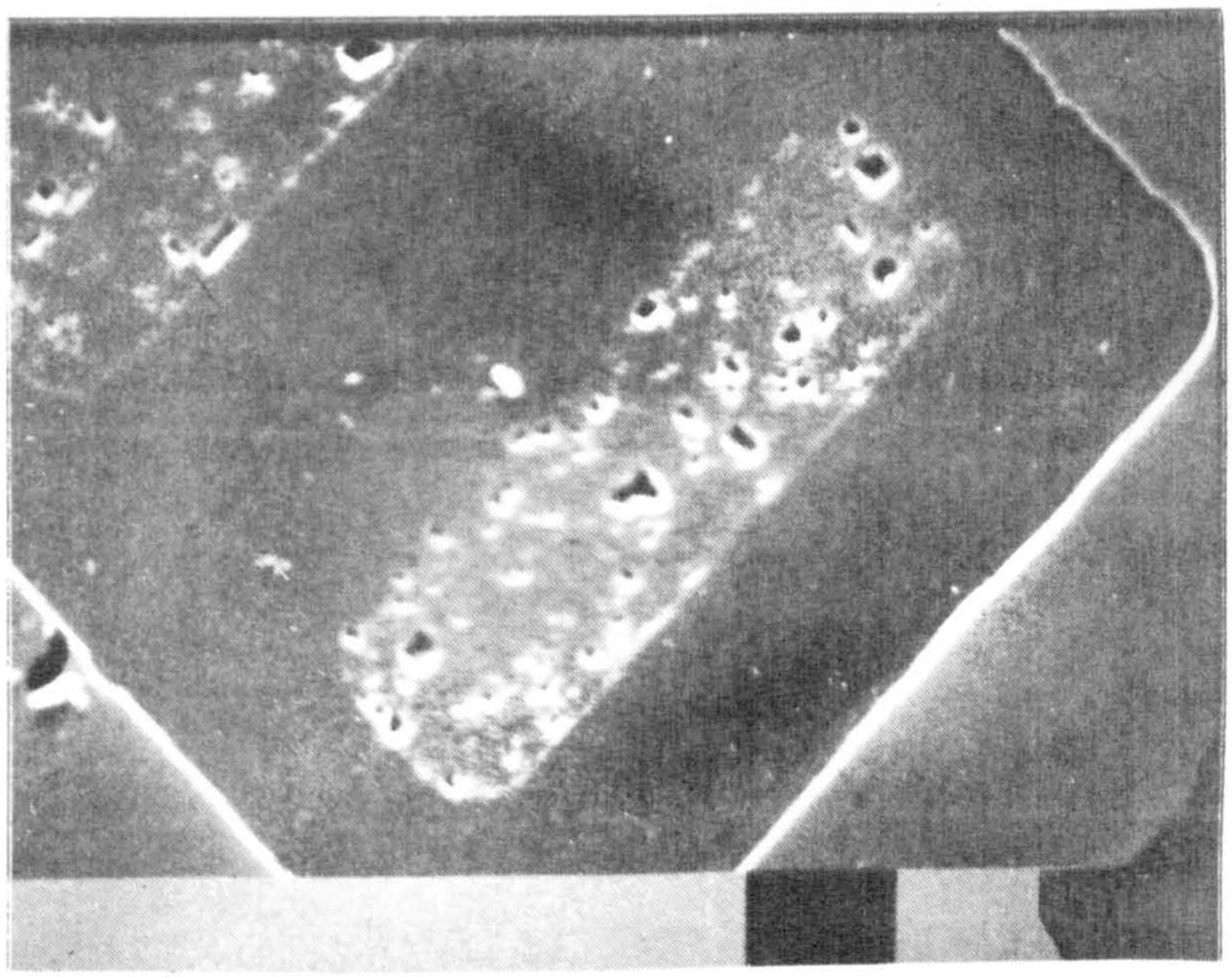


FIGURE 7.4 METALLISATION PITS (SEM)

(a) Metal edge (metal not removed)

(b) In contact (metal removed)

sinter and if the sinter is too severe the titanium is no longer an effective barrier. The second problem is pinholes in the titanium which can occur if the wafer surface is not properly cleaned. An analysis of early Process III I^2L samples showed that the metallisation system was inadequate for large area circuits, A small but significant number of devices failed due to shallow N^+ - base (emitter - base) short circuits. (< 5%)

The first approach to this problem was to reduce the sinter temperature from 500°C to 400°C. This was shown to cure the problem, contact resistance was a good as standard; however metal adhesion to the chip surface was poor and during bonding some pads lifted off the chip surface under a few grams stress. Increasing the sinter temperature to 425°C recovered the metal adhesion and eliminated shallow N^+ - base short - circuits. Contact resistance was identical to standard and a small sample on electromigration life test produced results comparable with standard processing.

7.2.4. Low-current gain (Sintering)

I^2L circuits and LSI circuits need to operate at low power if chip dissipation is to be minimised. In Bipolar transistors, gain (both βu and βd) decreases with decreasing collector current. This is due to depletion region recombination. The major component of this current in Process III is in the surface depletion region (See Appendix 1).

In a process using aluminium or silicon doped aluminium, the sinter increases gain in the following way. Protons released

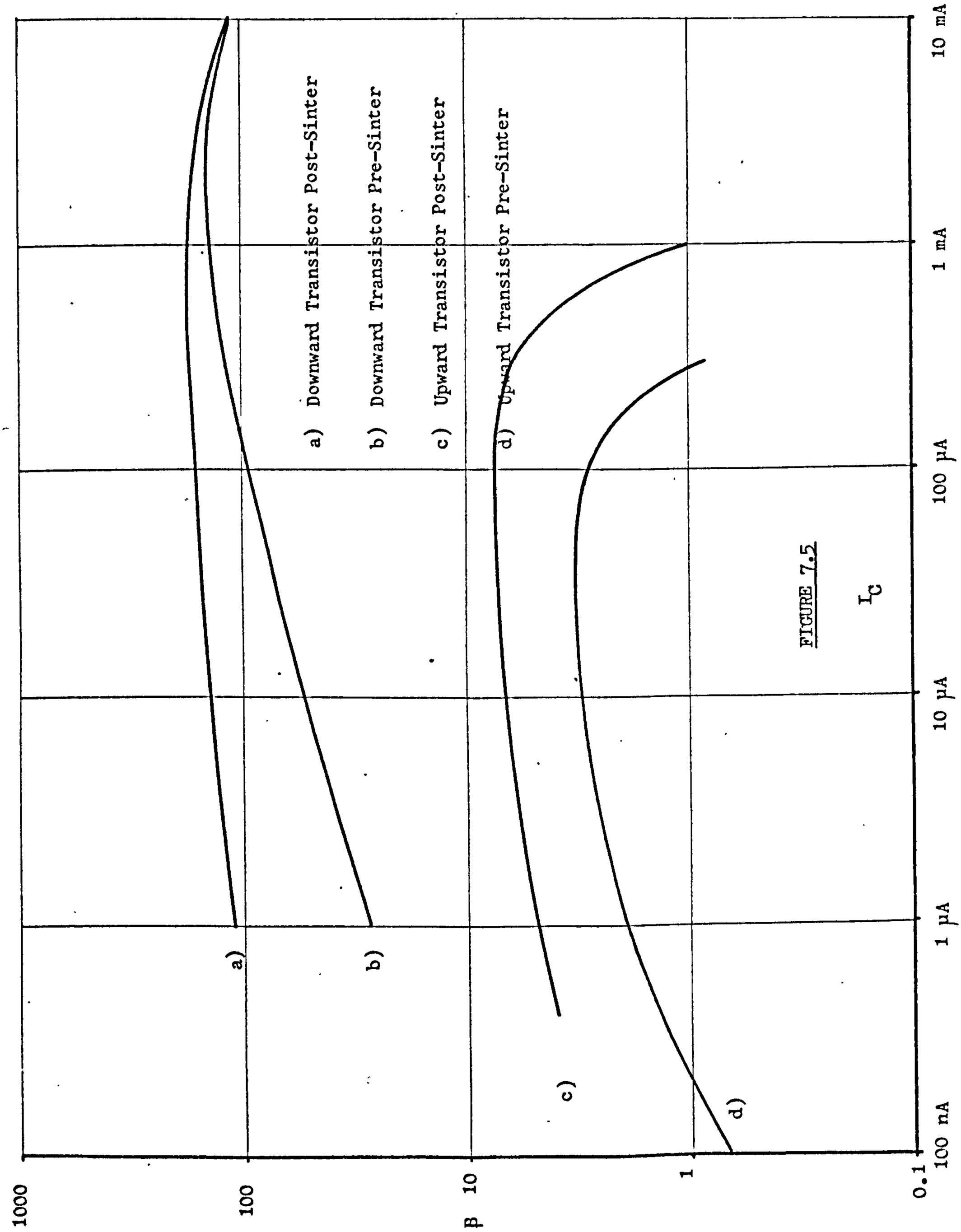


FIGURE 7.5 Effect of Sintering on Gain

from the water trapped in the passivating SiO_2 (by reaction of H_2O and aluminium) migrate to the Si/SiO_2 interface where they take up 'dangling bonds' which are responsible for the silicon surface states. With the titanium/aluminium system this cannot occur. Hydrogen may, however, be added to the sinter ambient. If this is done a marked improvement in gain is observed. Figure 7.5. shows results for 10% H_2 in N_2 (forming gas) anneal/sinter. The low current gain of the downward npn is clearly improved. For the I^2L gate there is a dramatic improvement in gain probably due to both a reduction in surface state density and/or an improvement in bulk lifetime values. Unfortunately this type of data is difficult to obtain. The effect of forming gas sinter on the lateral pnp transistor D.C. characteristics is shown in Chapter 5, section 2.

7.3. COLLECTOR-EMITTER LEAKAGE "PIPING"

7.3.1. Review of Pipe Phenomena

In a review paper Verhofstadt (3) stated that although projected yields on I^2L were very high this yield had not yet been demonstrated and the basic yield limiting characteristic of all bipolar processes in the form of emitter-collector shorts or leakage (pipes) has not been eliminated. Although this is a sweeping generalisation it has a considerable validity when applied to Process III. Measurements on other bipolar processes indicate that the pipe problem can be non-existent and that photoengraving is the major yield limiting phenomenium. A review of the understanding of pipes follows which is by no means complete but will serve to introduce the subject.

The formation of pipes in bipolar transistors has been attributed to a variety of mechanisms. The first reported observation of pipes was by Miller (4). He observed by bevel and stain techniques, small local n-type regions transversing the p-type base of his piped transistors.

He proposed as a mechanism of formation localised rapid diffusion of emitter (shallow N^+) dopant down a dislocation. Unfortunately this could only be a speculation as he had no means of proving his observation.

Goetzeberger (5) showed that pipes could be formed by particulate contamination of the wafer surface prior to shallow N^+ diffusion. In Goetzeberger's case the particulates were of phosphorus and his results suggested that P_2O_5 from emitter furnace exhaust was present in some airborne atomised form. In a modern diffusion facility conditions are carefully controlled to avoid this.

Jungbluth and Wang (6) made X-ray topograph observations on silicon epitaxial transistors and showed that transistors fabricated in regions of high dislocation density exhibited a higher incidence of collector base leakage. This leakage was attributed to diffusion pipes at the dislocations.

Although it had been demonstrated by Queisser et al in 1961 (7) that enhancement diffusion was possible along a crystal disorder (single angle grain boundary in this case) it was only with the development of better analysis techniques that evidence of individual crystal defects causing pipes emerged. By correlating bevel and stain results with previous observations of the position of stacking faults and slip dislocations, Barson et al (8) showed that pipes could be formed at the edges of epitaxial stacking faults and on slip dislocations. By a novel preferential etching technique Plantinga (9) was able to show a correlation between slip dislocation and pipes. In both the previous studies the correlation between defect and pipe was never 100%, probably because some form of precipitate is necessary at the defect to form the pipe. This conclusion was apparently verified by Parekh (10) who observed that increasing gold concentration in a saturating logic process increased pipe density. Pipes in this case were associated with epitaxial stacking faults and slip dislocations.

By investigating individual piped transistors using a transmission electron microscope (TEM) Tice et al (11) were able to show that pipes could be caused by a number of other crystal defects, viz. dislocation loops, epitaxial stacking faults, oxidation induced stacking faults, slip dislocations and individual dislocations. These can originate from the silicon wafer itself or be process induced.

Foll and Kolbesen have developed improved TEM techniques (12) and have verified most of Tice's observations. They were unable to show precipitates or decoration on large numbers of the defects which caused pipes. They showed that oxidation-induced stacking faults (OSF); which when delineated by preferential etching appear identical, differ markedly when observed by TEM. A variety of possible OSF structures were observed and they felt that the variation in electrical behaviour of transistors with OSFs in the shallow N^+ could be explained in this way. By examining piped transistors using sophisticated SEM techniques, Varker and Ravi (13) were able to obtain a good correlation with OSFs. Further, they were able to observe the development of the defect from base processing onwards. The mechanism postulated was the decoration of the defect with copper at base diffusion. Either the copper itself acted in some way to form the pipe or the copper was leached out at shallow N^+ photoengraving, leaving a void in the silicon in the region of the active base. Subsequent shallow N^+ diffusion would then penetrate the base causing a collector emitter short.

7.3.2. Slip Dislocation and Correlations with Yield

Observations of the positional dependency of transistor yield on Process III wafers showed quite clearly that crystal slip caused by process related thermal stress was a significant failure mechanism. (All the slices used in this study were 50 mm diameter, 450 μm thick except where stated).

Figure 7.6 shows a transmission X-ray topograph of a WM7 Process III wafer. The four lobe pattern of slip is characteristic of (100) oriented silicon (14). Material so slipped also shows a disordered region in the centre of the wafer which is also visible.

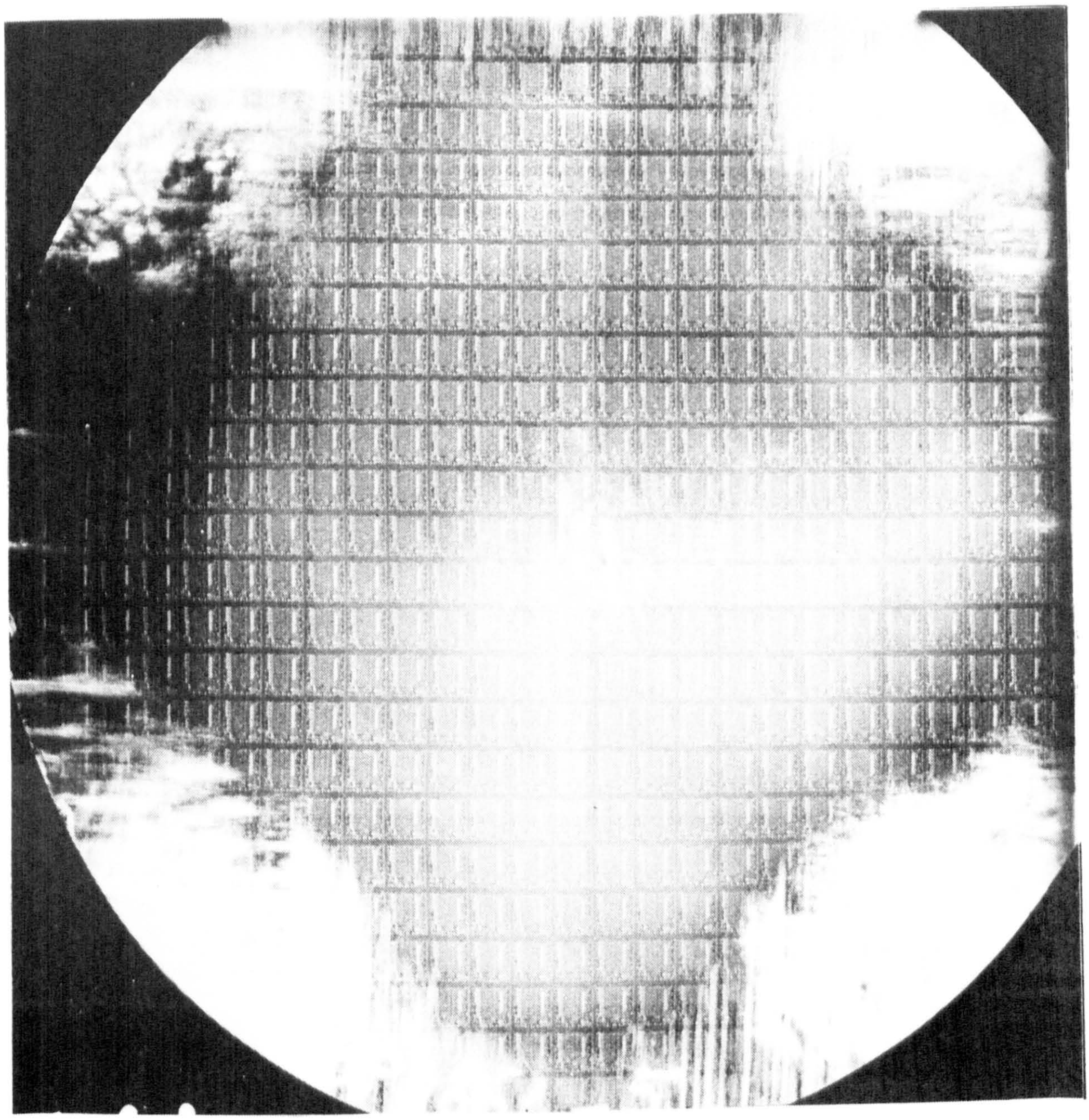


FIGURE 7.6 TRANSMISSION X-RAY TOPOGRAPH
PROCESS III WM7 WAFER

The WM7 mask set contains a test transistor and a test I^2L gate on each chip. Figure 7.7 shows a wafer photograph in which all the chip sites exhibiting collector-emitter failure on either the test transistor or test gate are identified by a dot. These failures point to a close correlation between slip and piping.

Using the dislocation etch described by Secco d'Aragona (15) (known as Secco etch) investigation of piped transistors in slipped regions showed dislocation etch pits in their shallow N^+ regions. Figure 7.8 shows a Secco etched piped transistor from a slipped region. The correlation between dislocation etch pit piping was 100%, provided the samples were prepared from slipped regions. Samples in these investigations were etched for six minutes, in which time approximately 9 μm of silicon was removed. The Secco etch is then delineating a dislocation approximately 8 μm below the emitter-base junction of the transistor.

As the Secco etch is dependent on the electrochemical potential in the silicon and hence the Fermi level, the etch rate in the active part of the transistor is controlled by the doping concentration. A simple dislocation offers only a point perturbation of the Fermi level in the shallow N^+ as it is heavily doped. Thus the dislocation is only delineated when the etch reaches a low doped part of the structure beneath the active regions.

The other etch pits observed outside the active area of the transistor in Figure 7.8 are due to slip dislocations which have intersected the wafer surface in low doped regions. These pits become enlarged during the etch period necessary to delineate the dislocation present in the shallow N^+.

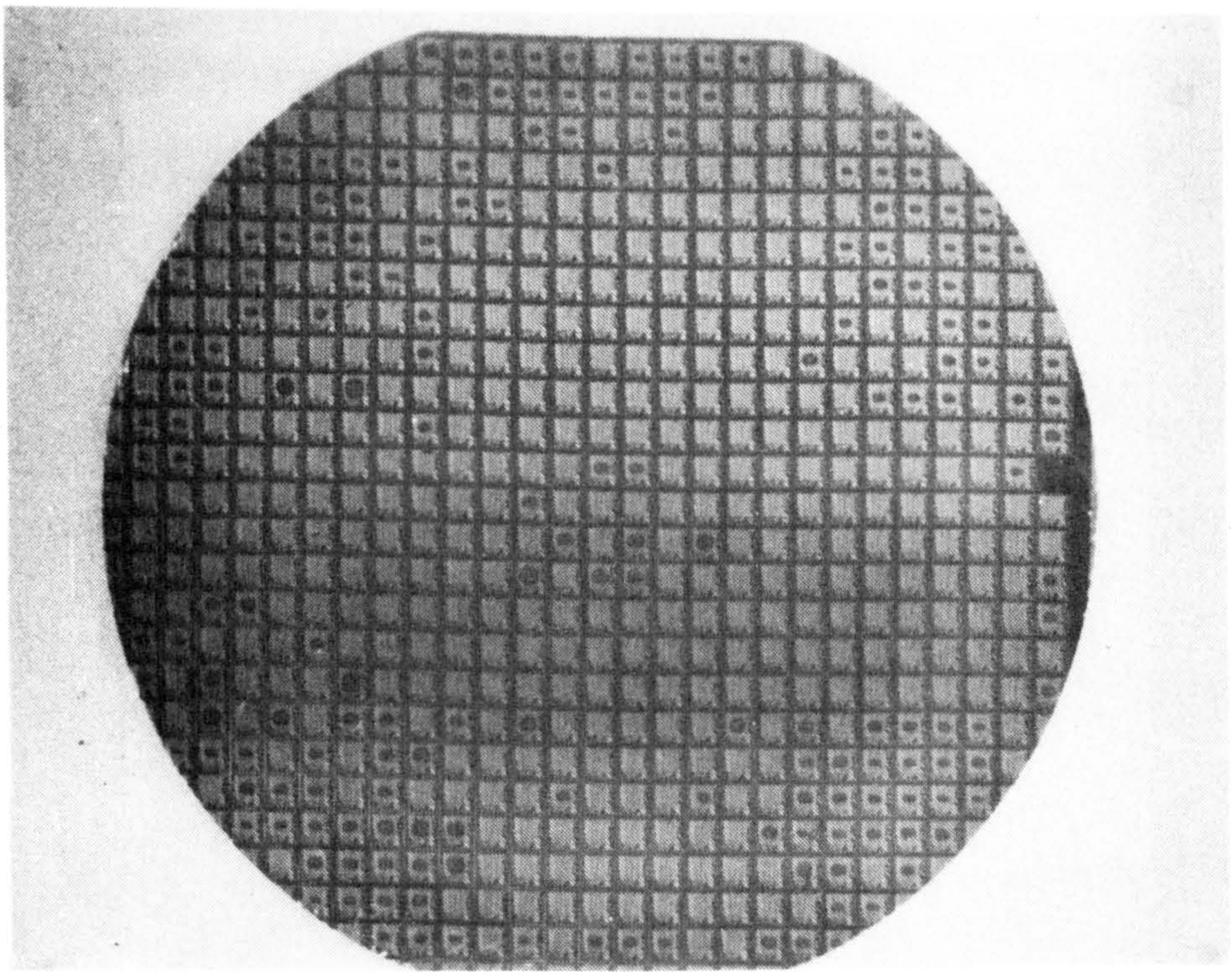


FIGURE 7.7 TEST TRANSISTOR FAILURES

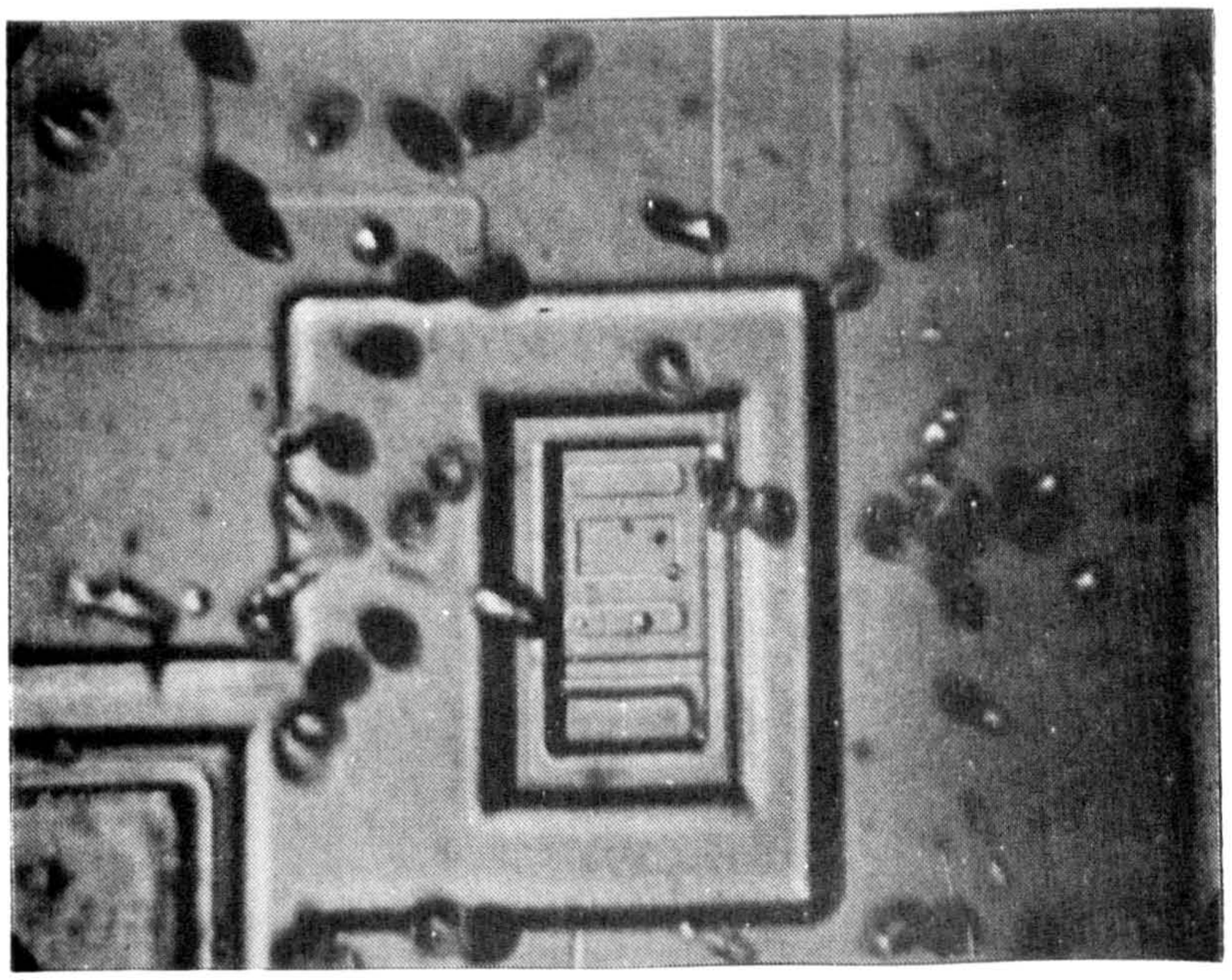


FIGURE 7.8 SECCO ETCHED PIPED TRANSISTOR

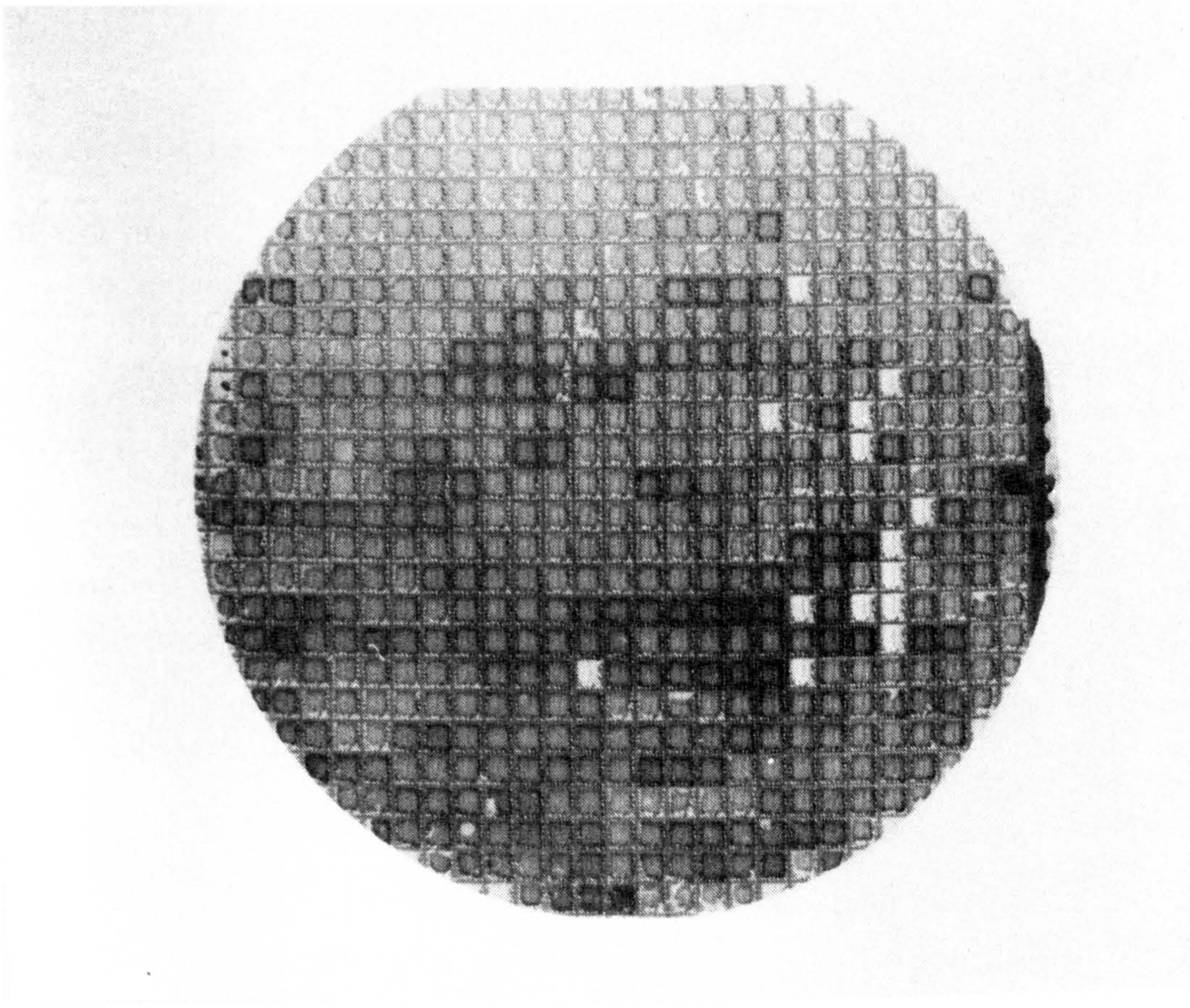


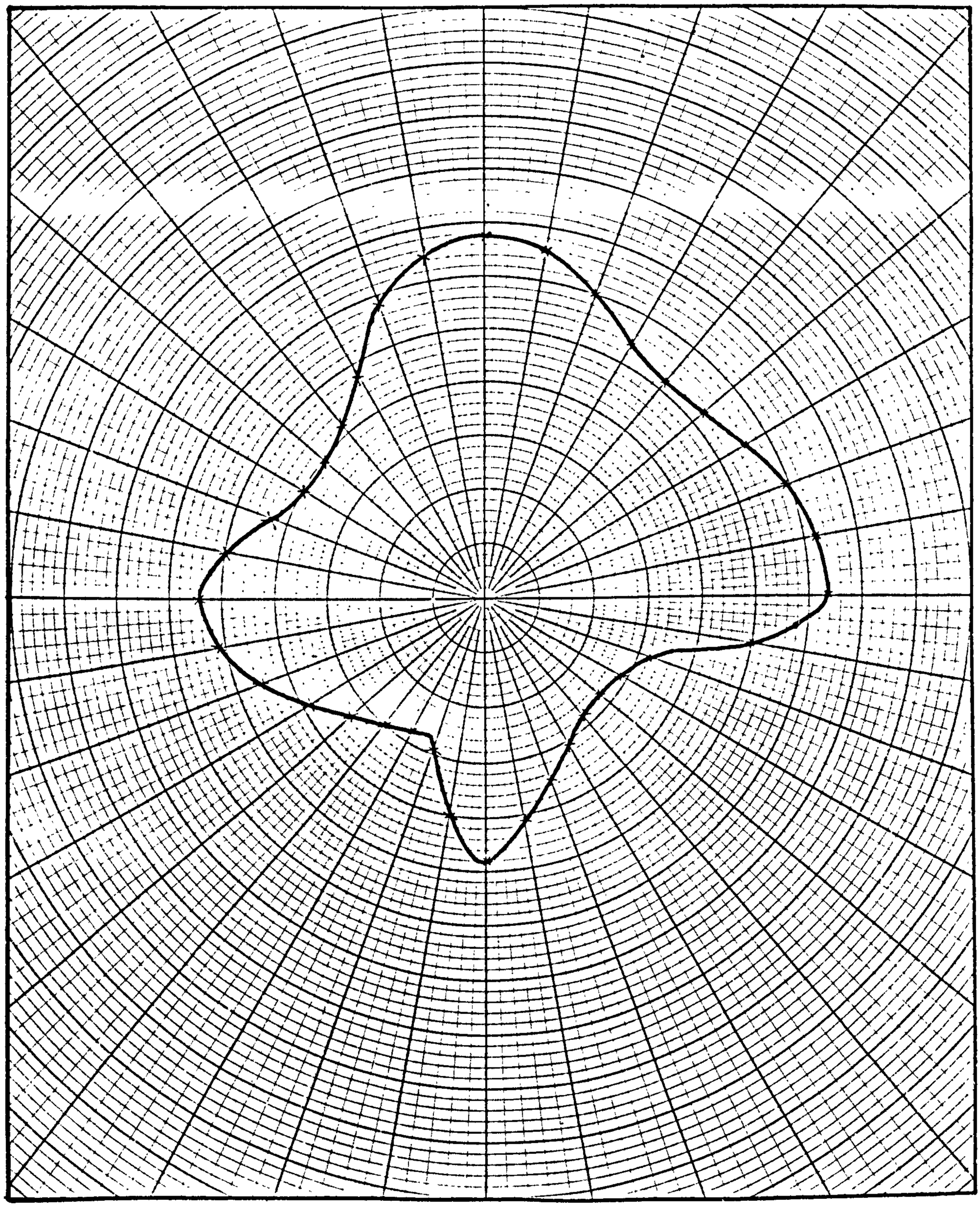
FIGURE 7.9 MULTIPROBE YIELD WM7 (EARLY BATCH)

(good devices are those lightest in colour)

FIGURE 7.10.

Angular dependence of Yield WM7

(Scale arbitrary units)



Flat

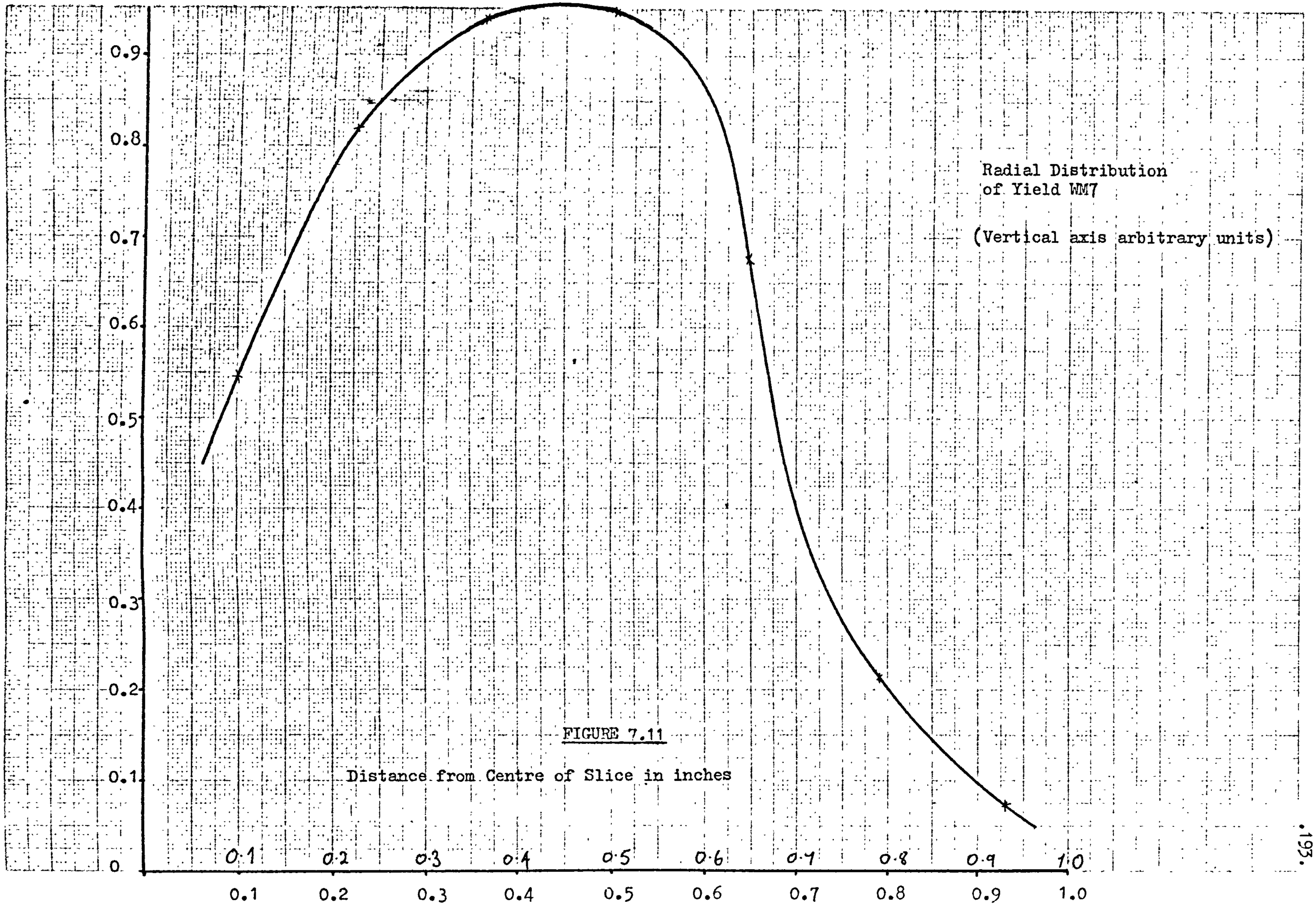

Radial Distribution
of Yield WM7
(Vertical axis arbitrary units)
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0·1
0·2
0·3
0·4
0·5
0·6
0·7
0·8
0·9
1·0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Distance from Centre of Slice in inches

FIGURE 7.11

A systematic analysis of the effects of slip on Process III has been carried out. Figure 7.9 shows the multiprobe yield of an I^2L circuit (WM7), all non-marked chips being good devices. On this sample, produced early in the investigation, there is no obvious positional dependence of yield. A similar observation on all wafers produced at this time would have shown this same result because yield was low. The positional information was obtained by accumulating the yield information from thirty wafers on a master wafer map. The data was then analysed in the following manner:-

(1) Angular Dependence

The master map was broken down into ten degree segments and the yield calculated as a function of angular displacement round the wafers.

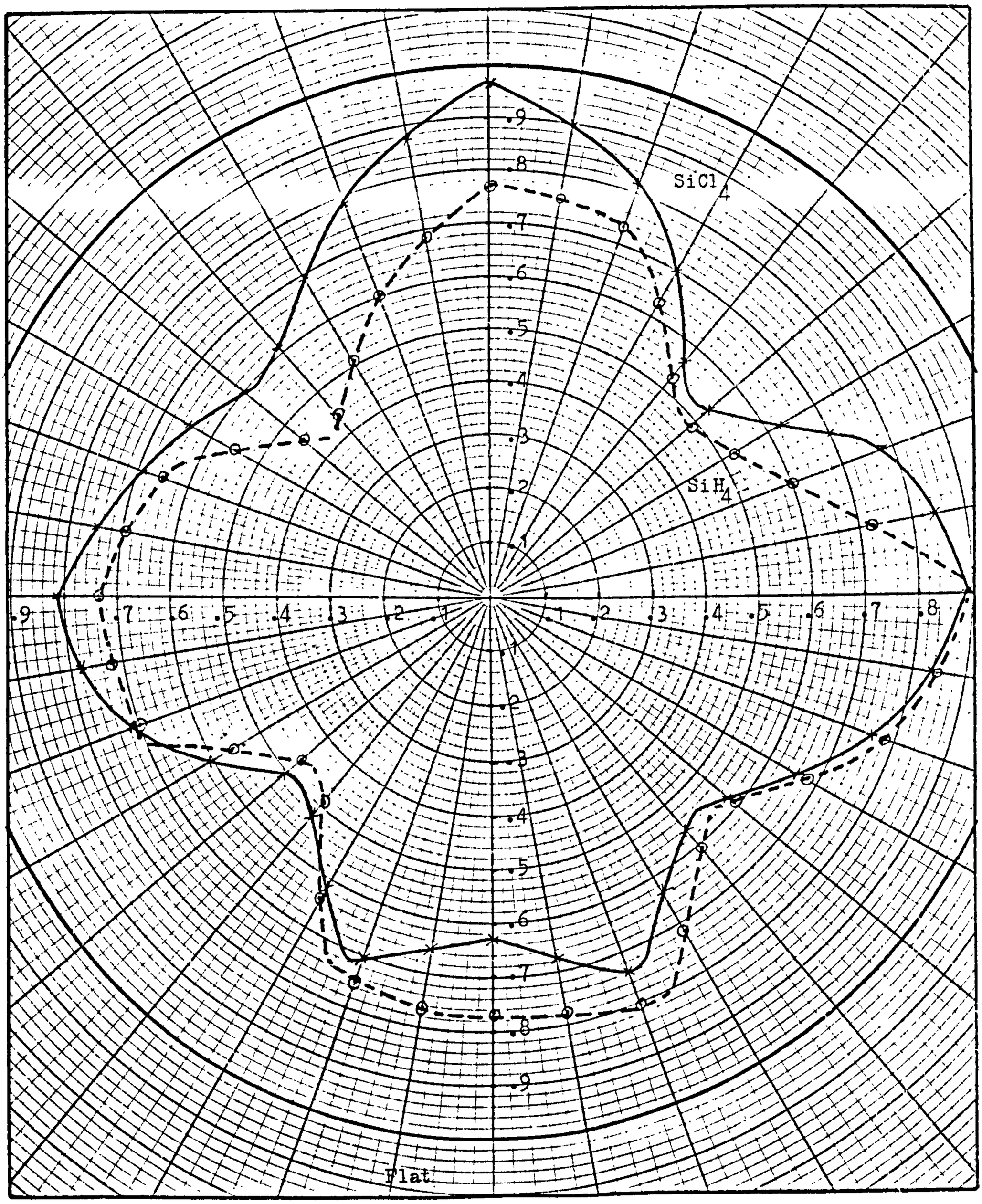
(2) Radial Dependence

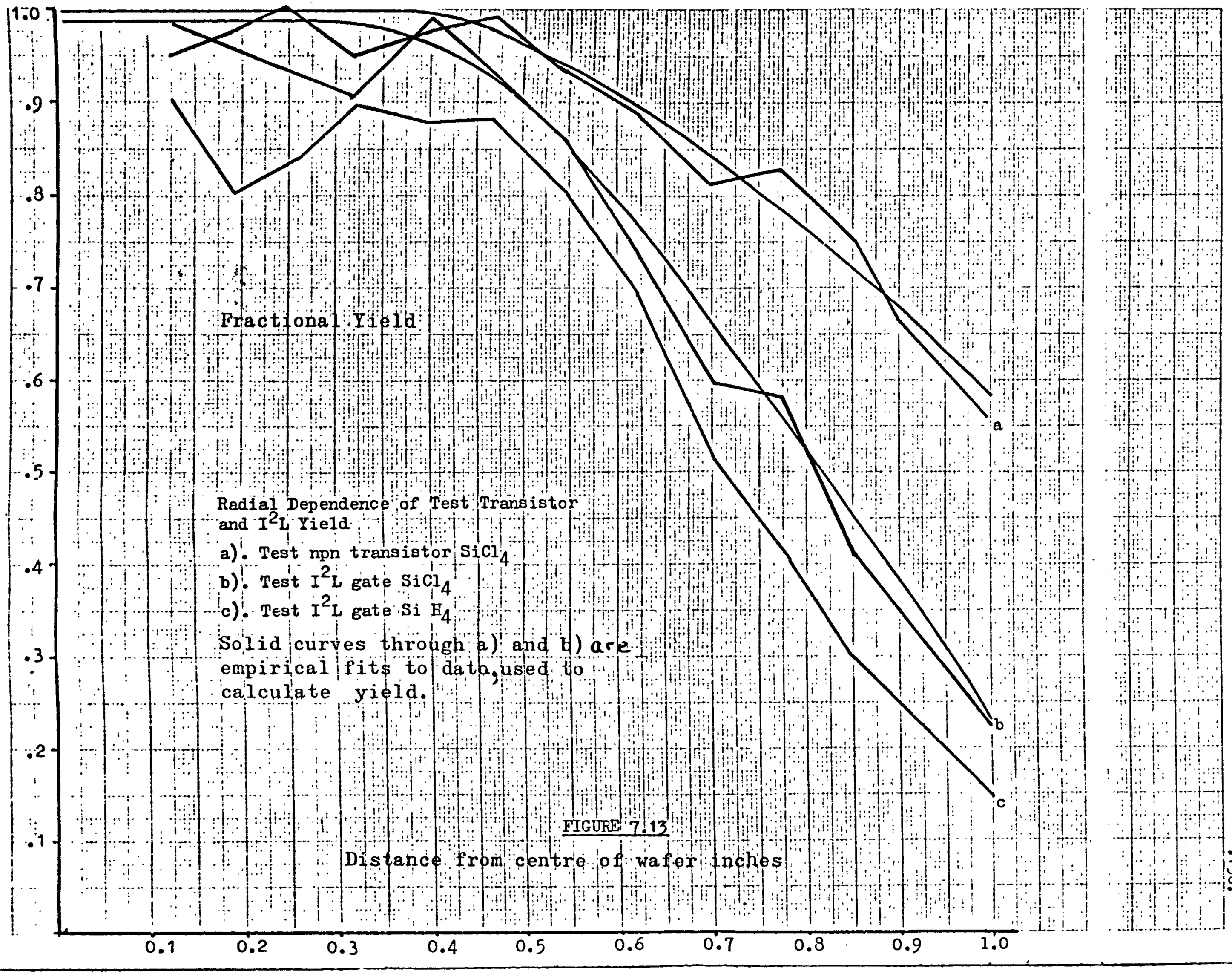
The master map was partitioned into annuli approximately two chips in width and the yield measured as a function of distance from the centre of the wafers.

The results are shown in Figures 7.10 and 7.11 respectively. These results show a strong dependence of circuit yield on the characteristic slip pattern. The angular dependence of yield is also shown to be affected by the silicon manufacturers' orientation flat, this being an extra source of slip dislocations. The radial dependence of yield also shows that the slip in the centre of the wafer affects yield. The high yield areas of the wafer are all those not exhibiting slip as shown in the X-ray topograph.

FIGURE 7.12

Angular Dependence of Test Transistor Yield





Radial Dependence of Test Transistor and I^2L Yield

a). Test npn transistor $SiCl_4$

b). Test I^2L gate $SiCl_4$

c). Test I^2L gate $Si\ H_4$

Solid curves through a) and b) are empirical fits to data, used to calculate yield.

FIGURE 7.13

A similar exercise was carried out on two samples of four wafers to analyse the positional dependence of test transistor and I^2L test gate yield. The two samples were processed identically except for epitaxy. One sample used a silicon tetrachloride system at 1200°C; the other sample used a silane system at 1000°C with a hydrogen pre-fire at 1180°C. The result for angular dependence of test transistor yield is shown in Figure 7.12. The slip dependence of yield is evident. (Note also the effect of the slip propagated from the wafer flat). Interestingly there appears to be an inferior yield with the silane epitaxy system. A comparison of the test transistor and I^2L gate yield is shown in Figure 7.13 which shows the radial dependence of yield. This also shows that the silane epitaxy appears to be inferior. The comparison of test transistor and I^2L gate yield shows that to a first approximation the yield at any given radius is proportional to the ratio of emitter diffusion (shallow N^+) areas. This implies that the probability of a slip dislocation being in the emitter of a transistor is proportional to its area.

7.3.3. Experiments to Reduce Slip

Slip is caused by thermal gradients in the silicon wafers during high temperature operations. These thermal gradients cause stress. When this is above a critical value ($\sim 10^8$ dynes/cm^2 at 1200°C to 4.5×10^8 dynes/cm^2 at 815°C (16,17)) slip dislocations are generated.

Penning (18) suggests that axial thermal gradients are not able to produce slip. In a simplified treatment Bloem and Goemans (19) calculate that radial temperature gradients of the order 10 degC/cm at 1200°C and 44 degC/cm at 815°C will cause slip on 2 inch silicon wafers.

An investigation of all Process III high temperature operations showed that those above 1000°C caused significant slip. These are:

1st Oxidation	1100°C
Buried N^+ Diffusion	1200°C
Epitaxy	1200°C (option of 1000°C silane)
2nd Oxidation	1100°C
Isolation Diffusion	1150°C
Deep N^+ (Collector) Diffusion	1100°C

Consider first the epitaxy; Figure 7.14 a, b and c shows transmission X-ray topographs of a sample of wafers processed through three types of epitaxial reactor: a Plessey silicon tetrachloride system, a Plessey silane system and a commercial system (Unicorp Inc. Unipac MK10). The commercial system undoubtedly produces the least slip. This system uses a large r.f. heated susceptor with a large thermal mass. Temperature gradients in the system are minimised. The inferior performance of the Plessey systems can be attributed to significant temperature gradients over the susceptors. One factor contributing to these temperature gradients is the relatively small dimensions of the susceptors, outer portions of the wafers being near to the susceptor edges where the heat losses are greatest and the inductive heating less efficient.

One problem with inductively heated susceptors is that slice heating is from the rear by physical contact with the susceptor. If there is a slight temperature gradient through the slice the front surface will be at a lower temperature than the back and will consequently expand less than the back surface, causing the slice to bow. The perimeter of the slice is then out of contact with the susceptor and cools, causing a radial temperature gradient and enough strain to slip the wafer. If an

FIGURE 7.14(a) TRANSMISSION X-RAY TOPOGRAPH
PLESSEY SILICON TETRACHLORIDE EPITAXIAL REACTOR

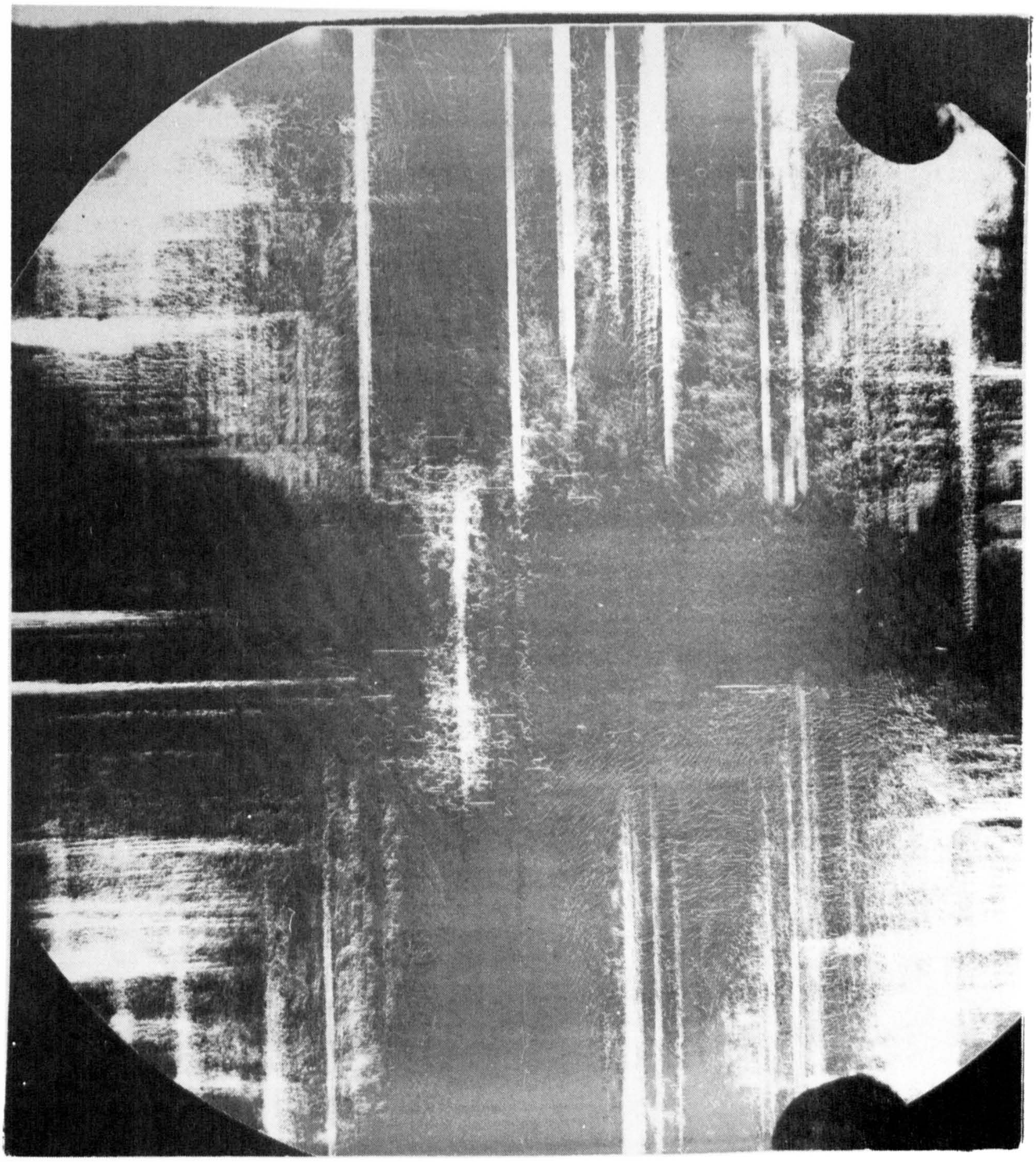


FIGURE 7.14(b) TRANSMISSION X-RAY TOPOGRAPH
PLESSEY SILANE EPITAXIAL REACTOR

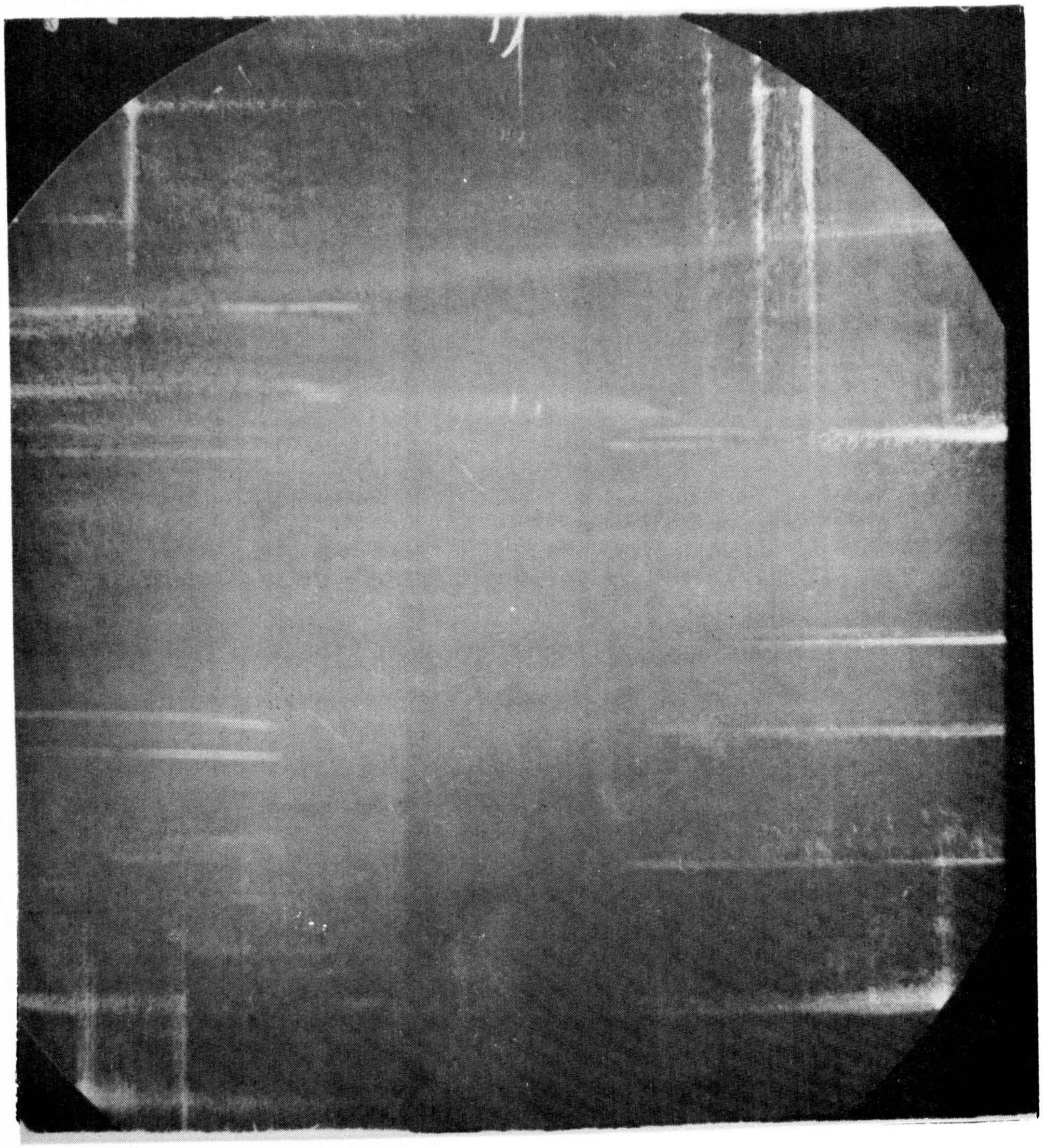


FIGURE 7.14(c) TRANSMISSION X-RAY TOPOGRAPH
UNICORP INC. UNIPAC MK10 EPITAXIAL REACTOR

extra susceptor is placed above the slices so that it is in a position to radiantly heat their top surfaces slip is reduced (20). Due to lack of suitable equipment this approach has not been tried at Caswell.

Commercial epitaxial reactors are now available in which infra-red radiant heating is employed rather than r.f. induction. These systems result in virtually zero slip during epitaxy. Evaluation of commercial systems showed that the Applied Semiconductor Materials 'Epilog 15-2' reactor was suitable for Process III. Figure 7.15 shows an X-ray topograph of a slice processed through the Epilog 15-2 reactor. The use of this machine has virtually eliminated slip at epitaxy.

Consider next the furnace treatments. Although the total elimination of slip in the high temperature furnace operations is not possible, it can be reduced to an acceptable level if the rate of change of slice temperature is minimised. Although both heating and cooling of slices has been discussed separately by various workers, both cause slip and both must be optimised if slip is to be minimised (21).

There are a number of possible methods for reducing the rate of wafer temperature change in furnacing operations:-

(1) The wafers are loaded and unloaded slowly from the furnace hot zone (21).

(2) The wafers are contained in a furnace jig of high thermal mass such that slice heating and cooling takes place slowly (22).

(3) The furnace hot zone is changed in temperature, i.e. load at low temperature ramp up slowly to working temperature and ramp down slowly on completion to unload temperature.

The first technique was that chosen for implementation on Process III I^2L.

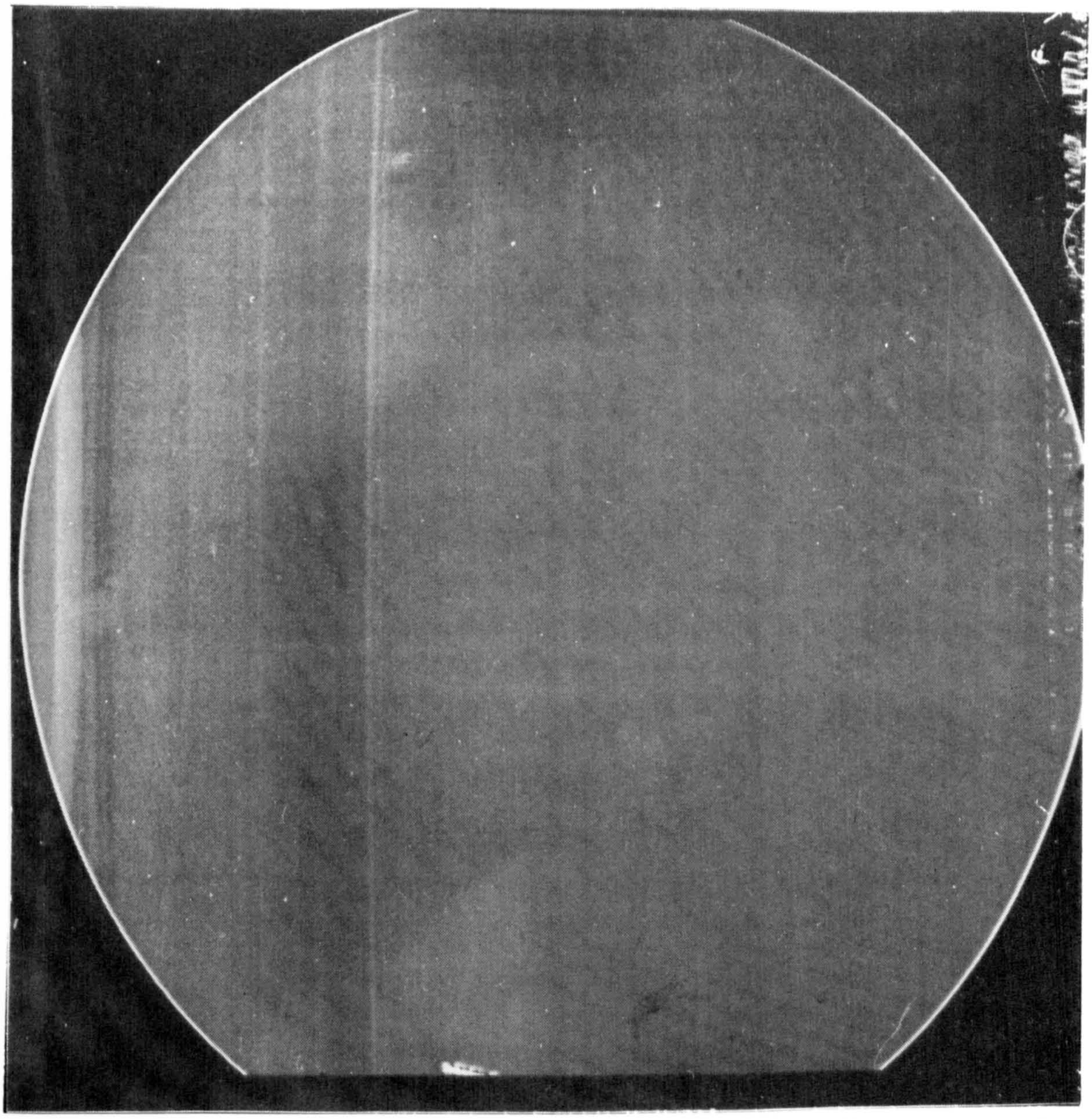


FIGURE 7.15 TRANSMISSION X-RAY TOPOGRAPH
APPLIED SEMICONDUCTOR MATERIALS EPILOG 15-2
EPITAXIAL REACTOR

The effect of varying loading and unloading rates, slice position in the boat and silicon type (float zone FZ, Czochralski CZ) was investigated. For furnace temperatures of 1200°C and above a load/unload rate of 3 cm per minute was found necessary to reduce slip to acceptable levels. For 1150°C and below 6 cm per minute is acceptable. Figure 7.16 shows X-ray topograph comparisons of Texas Instruments CZ material loaded into a 1200°C furnace six times. (Figure 7.16a, fast load/unload. Figure 7.16b, slow load/unload). Position in the furnace boat was found to be important, the wafers near the boat ends having slightly more slip than those near the centre. This is contrary to the information published in the literature (21).

A comparison of float zone and Czochralski slices showed that FZ material slipped appreciably more than CZ (Figure 7.17 a and b). This is related to the impurity content of the material. The slip in CZ silicon from different manufacturers was essentially the same and the slip in FZ from different manufacturers was also very similar.

A comparison of 300 μm and 450 μm thick CZ and FZ silicon slices showed that slice thickness had little effect on slip.

A further advantage of slow heating and cooling of the slices is that thermally induced slice warpage and bow is reduced. This simplifies some photoengraving procedures and generally makes slice handling easier.

7.3.4. Oxidation-Induced Stacking Faults (OSF) and Correlation with Yield

After an extensive programme to reduce slip it became evident that yield on Process III I^2L circuits had not increased significantly. Careful analysis of failed chips suggested that failure was still due to

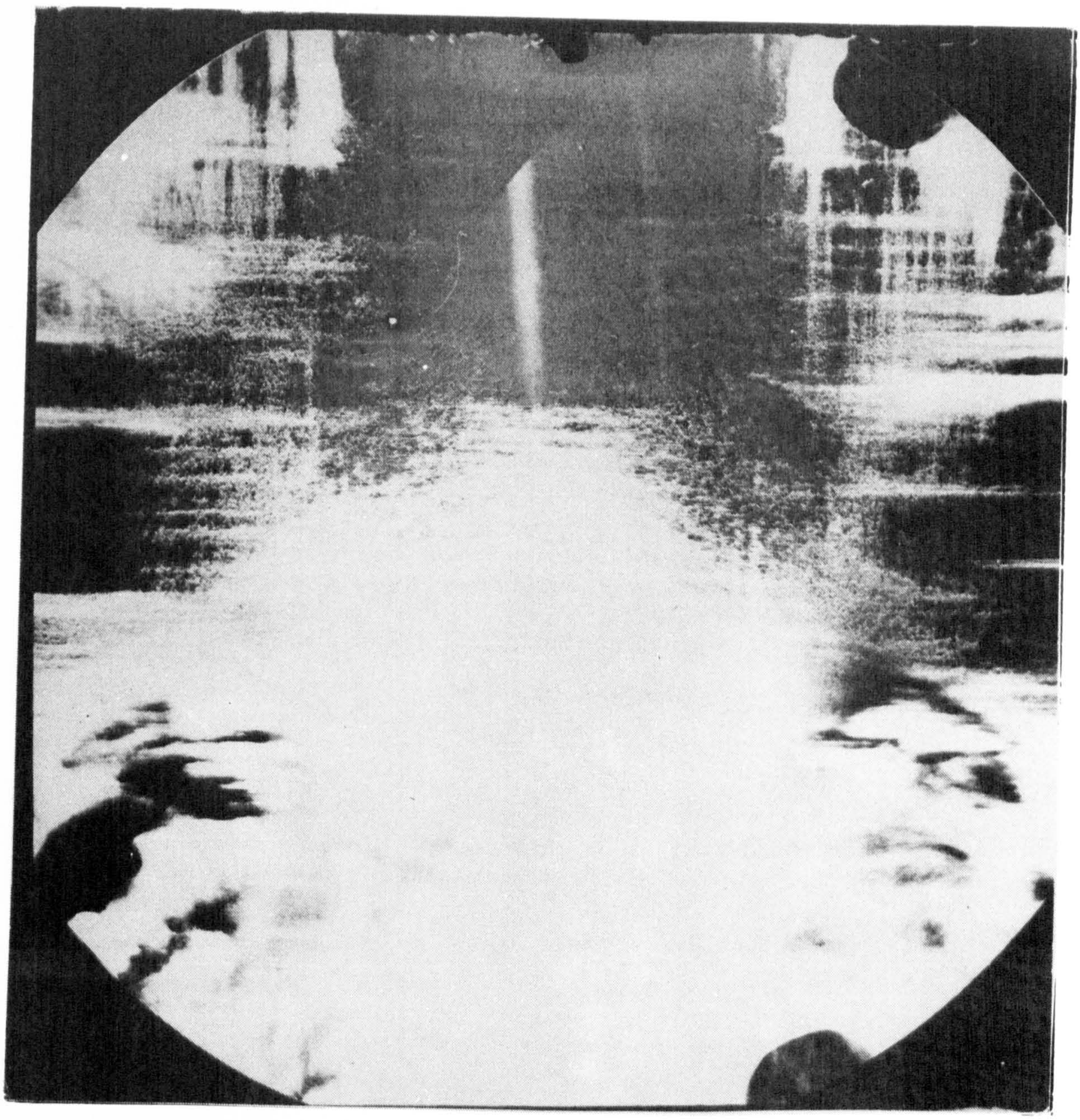


FIGURE 7.16(a) TRANSMISSION X-RAY TOPOGRAPH
TEXAS INSTRUMENTS CZ WAFER FAST LOADED/UNLOADED
SIX TIMES INTO FURNACE AT 1200^{o}C

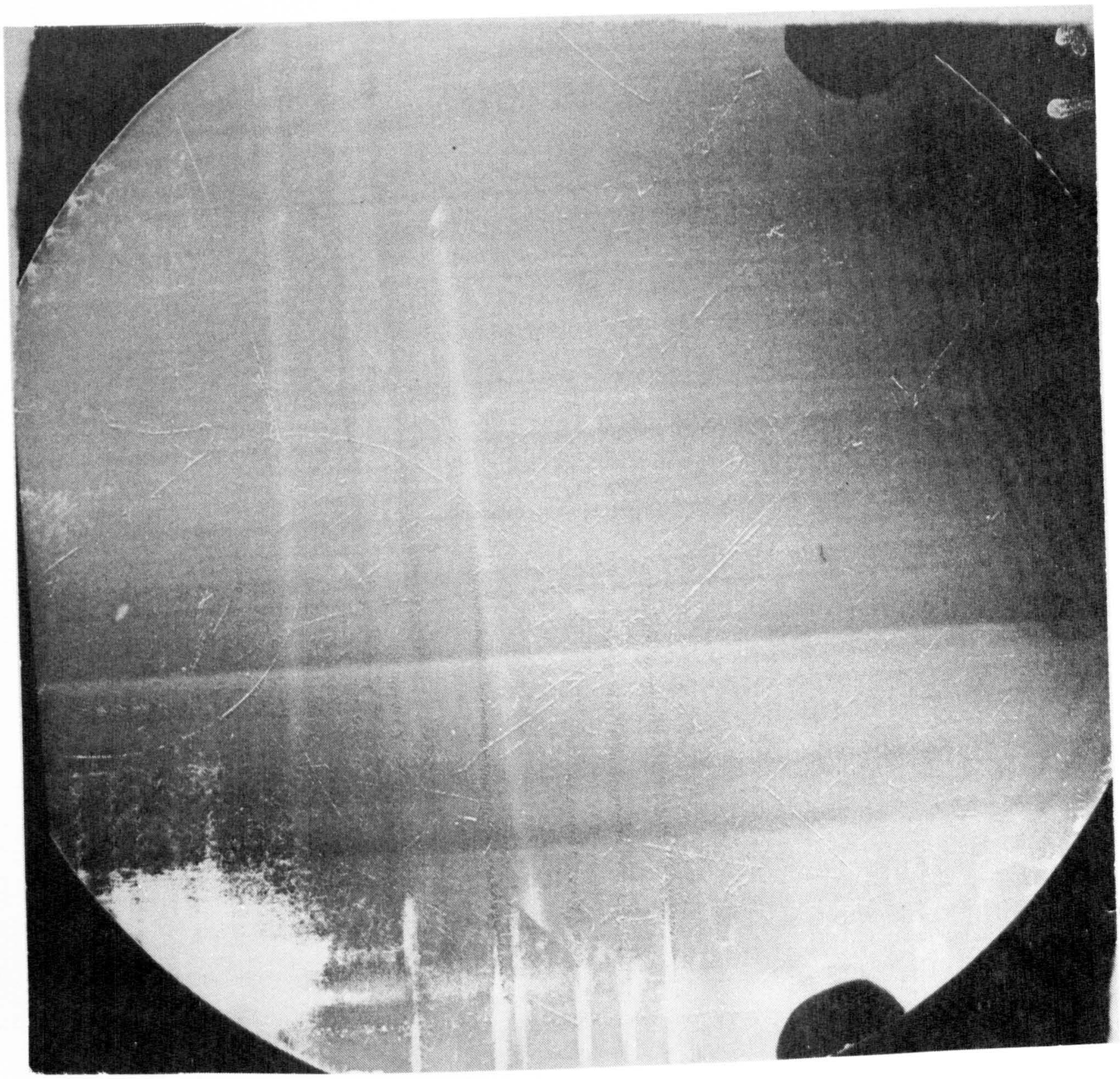
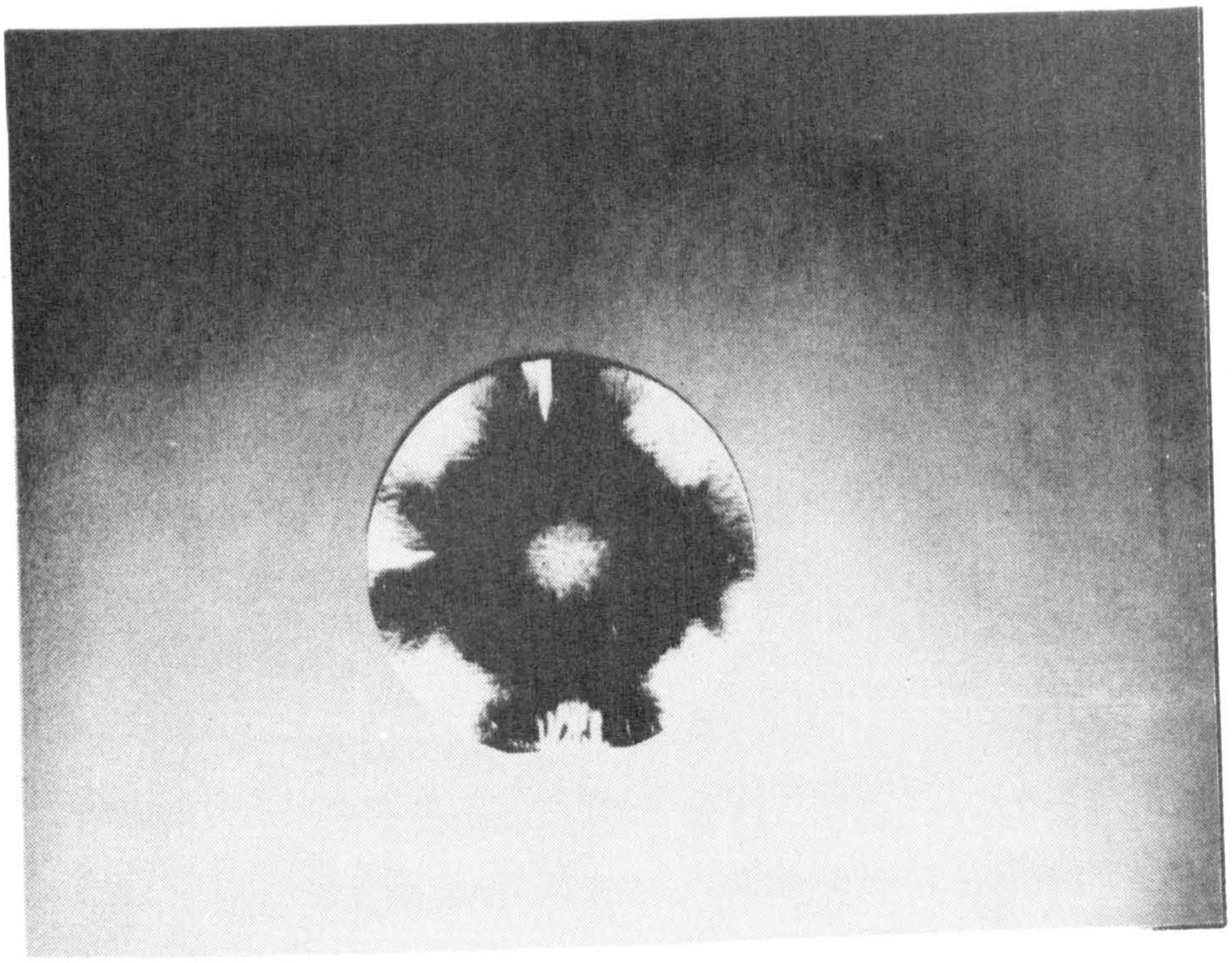


FIGURE 7.16(b) TRANSMISSION X-RAY TOPOGRAPH
TEXAX INSTRUMENTS CZ WAFERS SLOW LOADED/UNLOADED
SIX TIMES INTO FURNACE AT 1200^{o}C

(a)



(b)

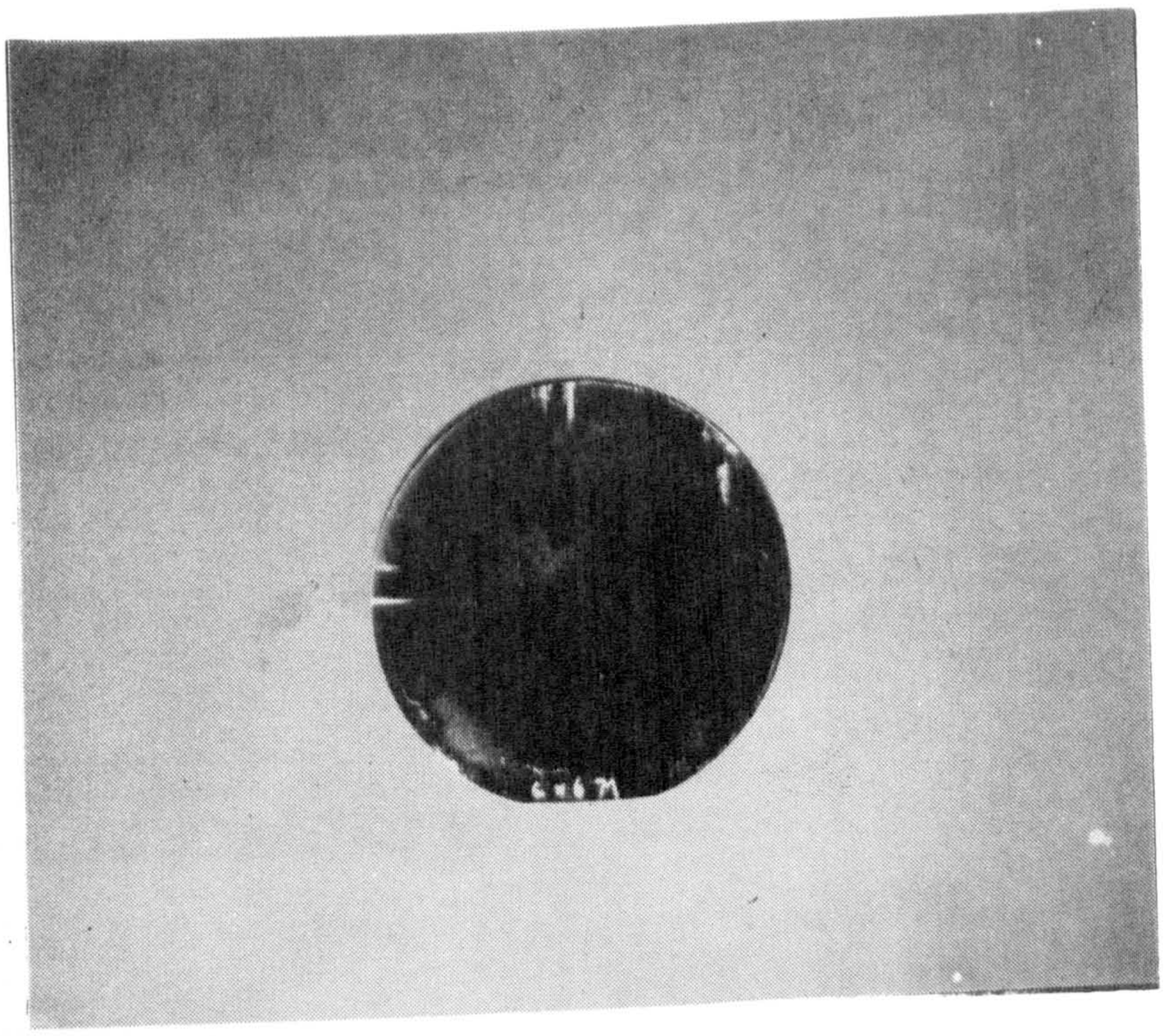


FIGURE 7.17 WAFERS SLOW LOADED/UNLOADED FOUR TIMES INTO A A FURNACE AT 1100°C.

Secco etched for 8 minutes.

(a) FZ

(b) CZ

collector emitter piping, the pipe characteristics being similar to those previously observed with slip. This piping had a very low incidence and was random over the entire slice surface. The position of piped transistors on a large number of wafers was mapped and the devices visually inspected. All samples with suspect photoengraving were ignored in subsequent analyses (< 1% of sample). Similarly, failures which could obviously be attributed to slip were ignored. The wafers were then stripped back to the silicon surface (that is, all oxide and metal removed) and given a one minute Secco etch. This short Secco etch revealed oxidation-induced stack faults. Table 7.1 lists the observed results. There is a high correlation between an OSF in the emitter of the transistor and pipes. Figure 7.18 shows a failed transistor with an OSF in its shallow N^+; note that an end of the OSF is within the emitter. Figure 7.19 shows an interesting anomaly; this transistor has an OSF passing through the shallow N^+. This device is not piped. With this fault structure it is probable that the partial dislocation bounding the OSF does not pass through the active base of the transistor.

A further exercise on a separate lot of wafers was to correlate failure rate with OSF density. Figure 7.20 shows a plot of transistor failure rate (pipe rate) against OSF density. From these results there appears yet a further link with OSFs and pipes. With OSF densities greater than 10^4 cm^{-2} the density of the ends of the faults is such that they appear uncorrelated, i.e. a single OSF can be considered as two independent point defects. (The OSF length is greater than average shallow N^+-shallow N^+ distance). If 'D' is OSF density and 'a' the shallow N^+ area, and locally on a wafer the OSFs are distributed uniformly then the probability of a defect occurring in an emitter is 2Da. This is the same as the pipe probability. The relationship in

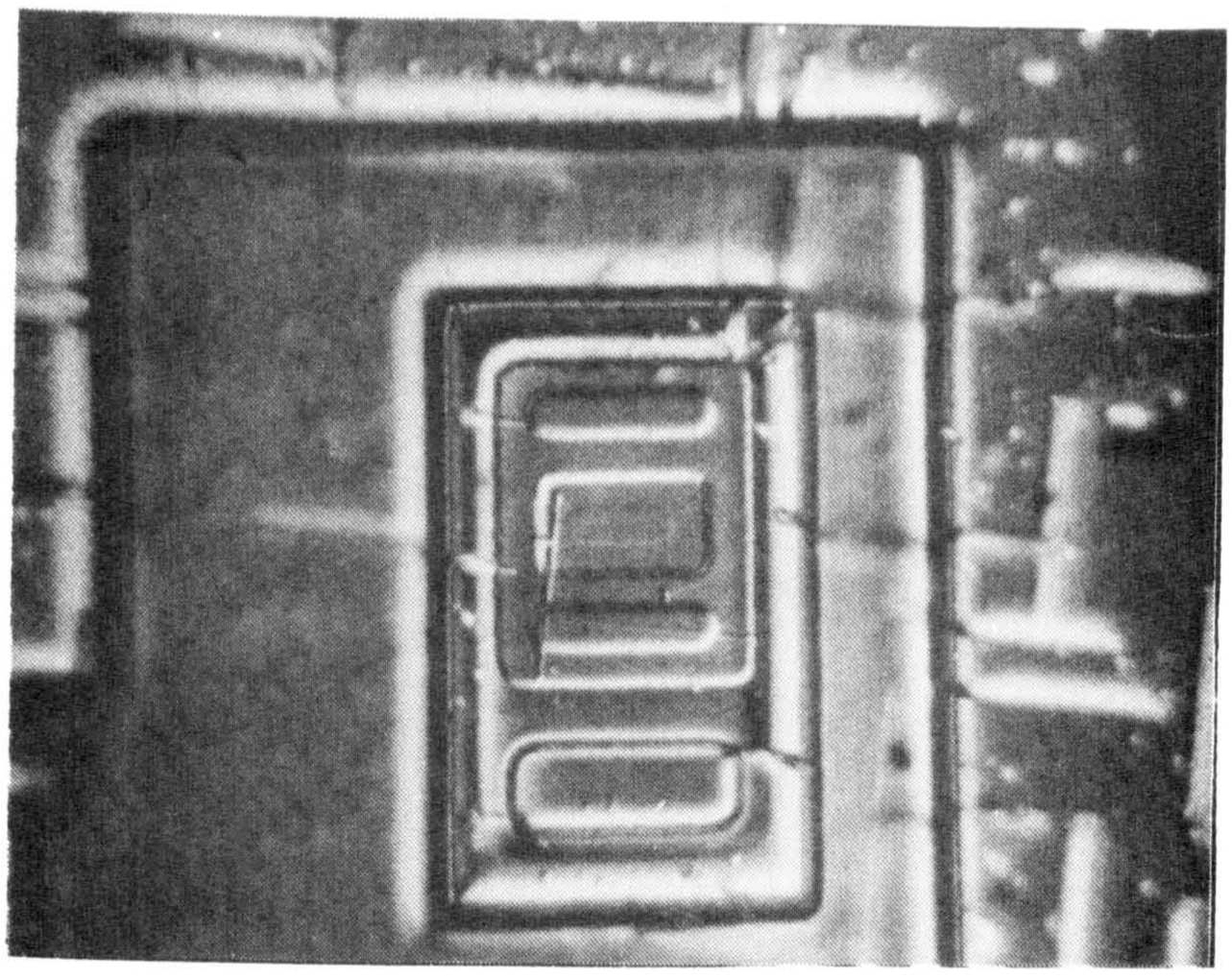


FIGURE 7.18 PIPED TRANSISTOR WITH OSF
(Normarski X650)

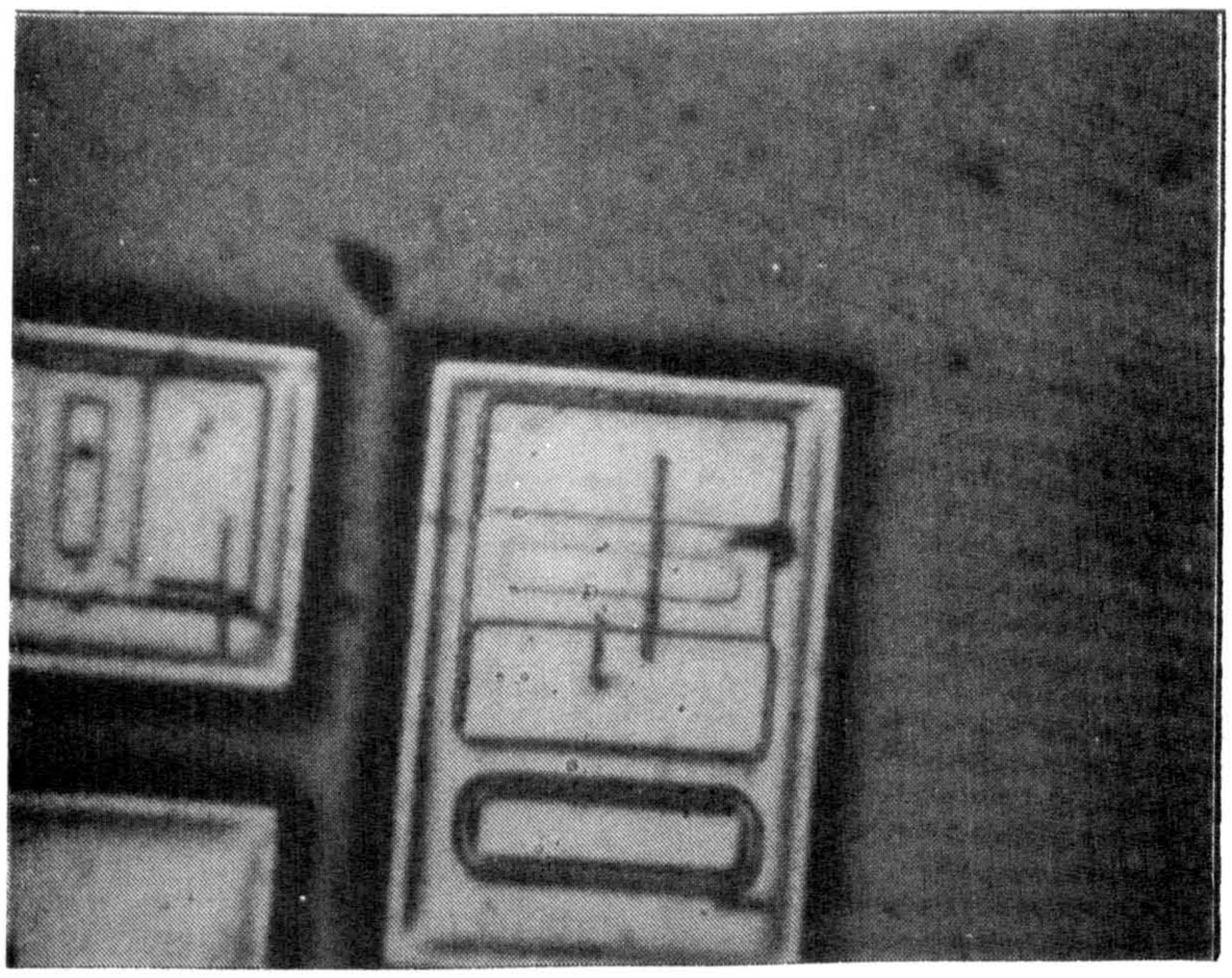


FIGURE 7.19 GOOD TRANSISTOR WITH OSF
(Normarski X650)

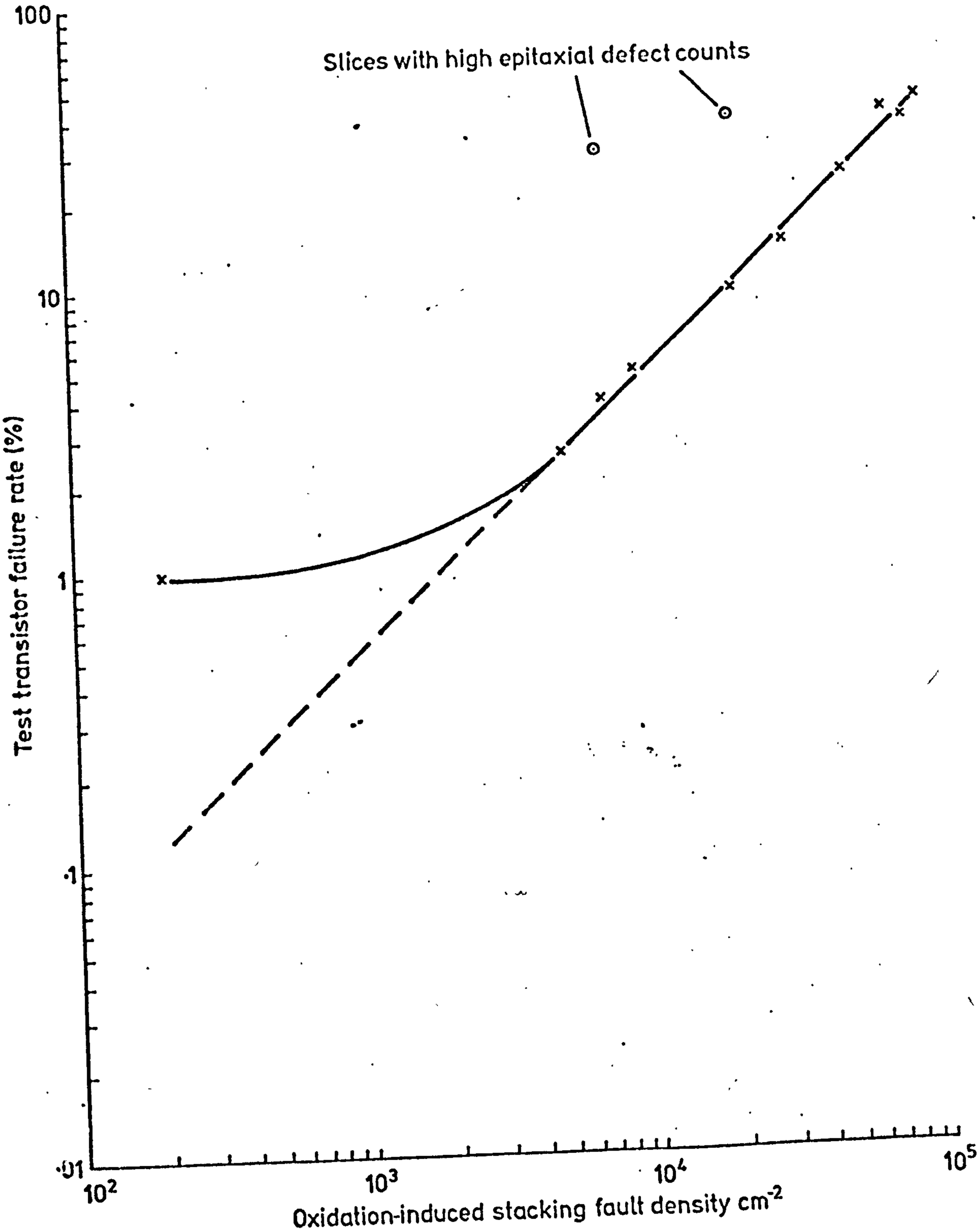

Slices with high epitaxial defect counts
100
10
1
·1
·01
Test transistor failure rate (%)
10²
10³
10⁴
10⁵
Oxidation-induced stacking fault density cm⁻²

FIGURE 7.20

TABLE 7.1.

SAMPLE SIZE 500

	NO.WITH OSF	NUMBER WITHOUT OSF
130 failed	95	35
370 passed	21	349

Figure 7.20 is approximately pipe density = 2Da.

Obviously an exact one to one correlation has not been observed. This may be because the pipe is not caused by the OSF but the pipe and OSF are produced by a common phenomena and both can be produced independently. An alternative explanation is that other pipe mechanisms are present at much lower levels. Edge dislocations for instance do not delineate in a short Secco etch.

Samples of failed devices were prepared for TEM analysis. These samples showed OSFs in shallow N^+ regions (Figure 7.21). Investigation of OSF length against depth showed that a 5 μm long OSF and a 20 μm long OSF would penetrate 1 and 3 μm TEM foils respectively. The OSFs under investigation all had depth to length ratios of the order 1:4. This ratio is such as to ensure that the OSF in Figure 7.19 passed under the active base of the transistor.

In the TEM investigations of fully processed wafers which had piped transistors, none of the observed OSFs showed any signs of decoration or precipitation. This is not to say that decoration or precipitation was not present but if they were they were below the threshold of detectability.

Analysis of multiprobe yields showed a clear correlation between yield and OSF density, no significant yield being observed on wafers with OSF densities of greater than 3×10^3 cm^{-2} on the I^2L circuit WM7. The best yield (25% for WM7) was observed with OSF densities of less than 100 cm^{-2}.

On the basis of the assembled evidence an extensive programme to investigate OSF nucleation and growth mechanisms was begun. The aim

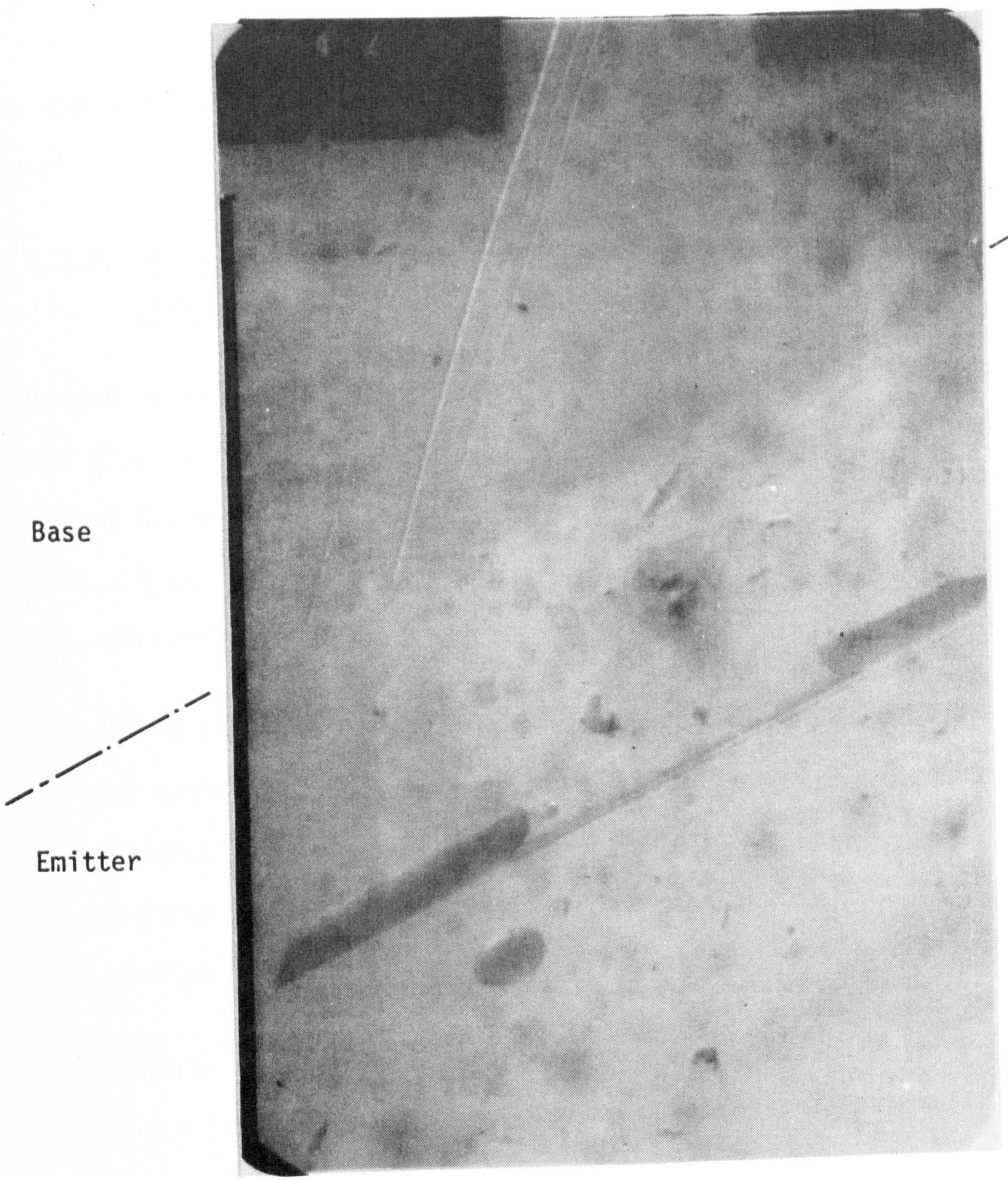


FIGURE 7.2 1. TEM PIPED TRANSISTOR CONTAINING OSF (X5.5K)

of the work was the total elimination of OSF as a yield limiting mechanism.

7.3.5. Oxidation-Induced Stacking Faults : Nucleation and Growth

Oxidation-induced stacking faults were first observed in silicon by Thomas (23) in 1963. Since this publication the list of papers on the subject has grown very large. Most publications only deal with OSF growth and shrinkage and only a few authors have studied nucleation or device effects.

The OSF in silicon is an extrinsic stacking fault bounded by a Frank partial dislocation (24). The stacking fault may be formed by the dissociation of a small initial perfect dislocation loop into Schottky and Frank partial dislocations. The Schottky partial glides out of the surface leaving the fault bounded by the Frank partial.

Observations by Ravi and Varker (25) suggest that the fault nucleates by the "local collapse of excess interstitial atoms" into a Frank dislocation loop. Patel (26) states that the probable nucleation of the OSF is due to a local excess of interstitials due to displacement of silicon by a precipitate. These excess interstitials diffuse away from the precipitate and collapse to form an extrinsic fault, i.e. a dislocation loop bounded by a Frank dislocation.

The OSFs observed are of two types, surface nucleated and bulk nucleated (that is, nucleated below the silicon surface). The surface nucleated OSFs have been shown to arise from mechanical damage, contamination, ion implantation damage, swirl (27) and point defects in the silicon (27,28). Bulk nucleated OSFs are probably due only to swirl

or point defects in the silicon. The growth of OSFs is very dependent on oxidising ambient and silicon orientation. A number of workers have published relationships between OSF length oxidising ambient, oxidising time and temperature. For the oxidations carried out in this study the following expressions due to Murarka and Quintana (29)

$$L_S = 4.92 \times 10^4 \; t^{0.66} \exp(-2.37 \text{ eV/kT})$$

$$L_D = 5.3 \times 10^4 \; t^{0.85} \exp(-2.55 \text{ eV/kT})$$

fit the observed OSF lengths. L_S applies to steam oxidations and L_D to dry oxidations. t is the oxidation time and T is the oxidation temperature.

Hu (27) has observed OSF shrinkage (retro-growth) after prolonged oxidation at high temperature (> 1200^{o}C). Unfortunately this kind of heat treatment is not acceptable for Process III.

In order to understand the formation of OSFs on Process III a number of experiments were performed using standard 5 Ω cm p-type CZ material. The wafers were oxidised and then Secco etched. OSF densities of approximately 10^2 to 10^5 cm^{-2} were observed in swirl patterns on most of the wafers. Wafers from the same lot were then processed through epitaxy and then given the Process III post epitaxy oxidation. After oxide removal and Secco etch (using only a light etch to ensure that no defects at the epi-substrate interface were delineated) OSFs were again found to be present in swirl patterns (Figure 7.22). This implies that the swirl pattern in the starting material had transferred through the epitaxial layer to cause surface nucleated OSFs. The swirl defects are thought to be oxygen-vacancy complexes. Pearce and Rozgonyi (30) established a clear correlation between interstitial

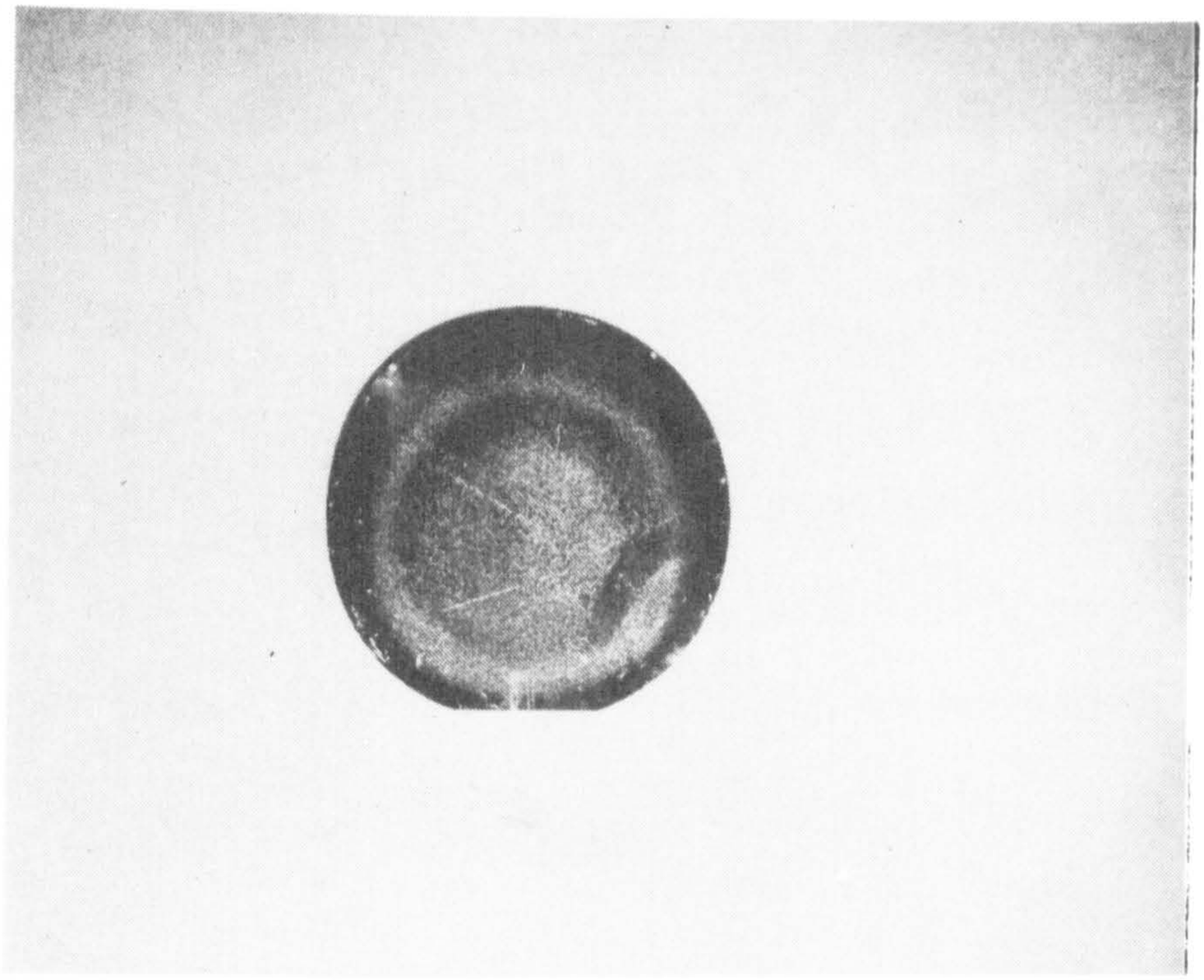


FIGURE 7.22 "SWIRL" - 1 MIN. SECCO ETCH AFTER POST EPI OXIDATION
(1 Hr. 1100^{o}C Steam)

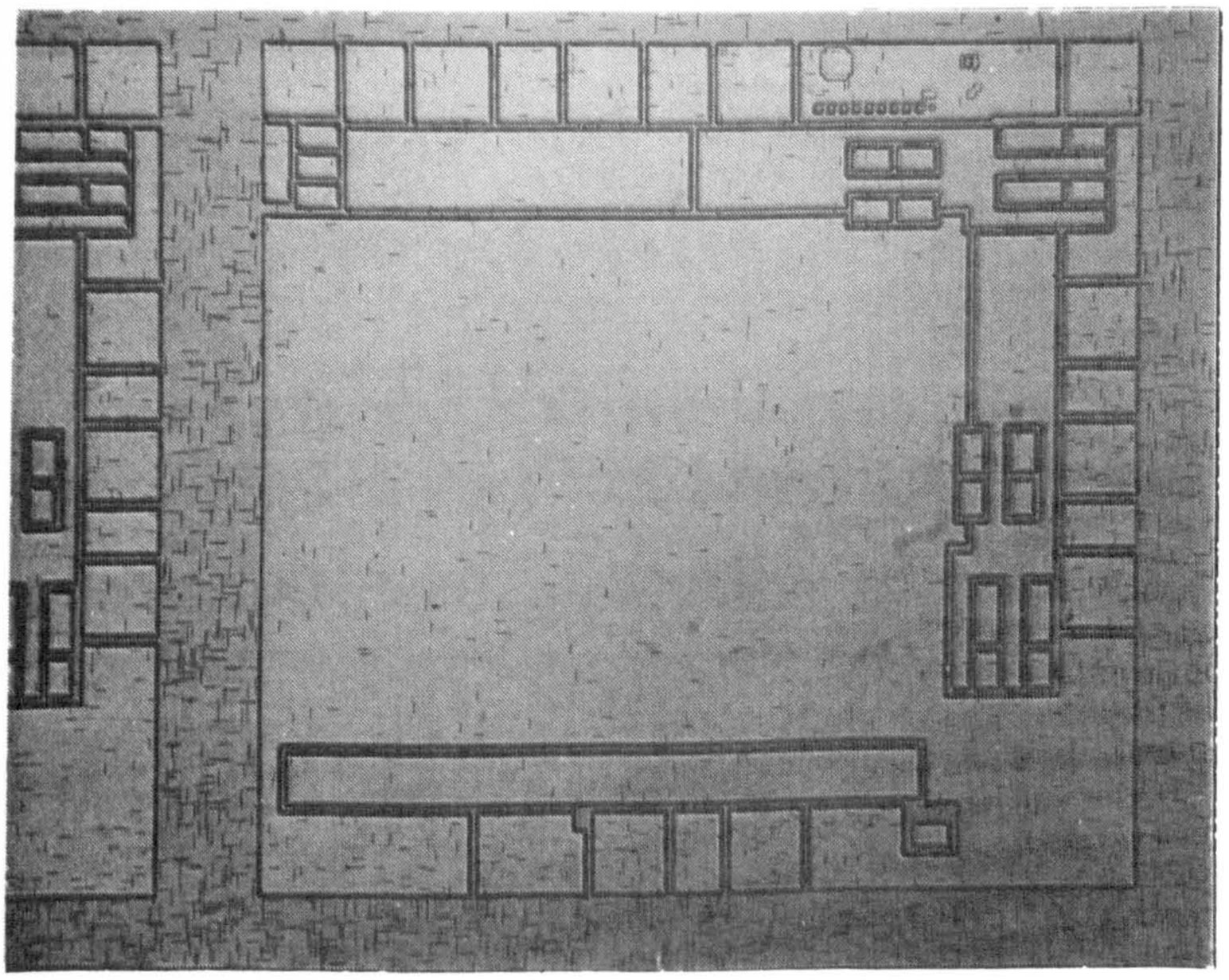


FIGURE 7.23 FULLY PROCESSED WAFER WITH ONLY BURIED N^{+} AND ISOLATION PHOTOENGRAVING OSFs IN HIGHEST DENSITIES IN ISOLATION DIFFUSED REGIONS
1 MIN. SECCO ETCH

oxygen content and OSF density. Oxygen content must be below 1.5×10^{18} at cm^{-3} to ensure a low OSF density from this mechanism.

Using a matrix experiment it was established that OSFs could be preferentially nucleated over buried N^+ (arsenic) diffused areas and that OSF densities tended to increase towards isolation diffused regions (Figure 7.23). OSFs tended to grow at the following operations only:

(1) Post epi oxidation (2nd oxidation)

(2) Isolation drive-in

(3) Collector drive-in

By a series of fortunate experimental results a number of further process steps of importance were discovered which affect OSF densities. Stainless steel contamination from tweezer handling was found to be of great importance. Figure 7.24 shows a wafer which had been lightly scratched (more correctly wiped) across the back surface with stainless steel tweezers in a cross pattern. The wafer was then oxidised and Secco etched for one minute. The figure shows the front surface of the wafer after Secco etch. The cross pattern visible is OSFs, a replica of the back surface marking. The contamination has diffused through the wafer and nucleated OSFs on the front surface. Cleaning experiments showed that a sulphuric acid hydrogen peroxide clean was unable to remove this contamination, but a hydrochloric acid hydrogen peroxide clean, or a nitric acid hydrochloric acid clean would. Normally after "acid peroxide" or "acid cleans", wafers are rinsed in high purity water (> 10M Ω cm), spun dry and then processed. With batches of wafers too large to clean in one operation the first part of the batch is usually stored in the furnace jig placed in a quartz container. As

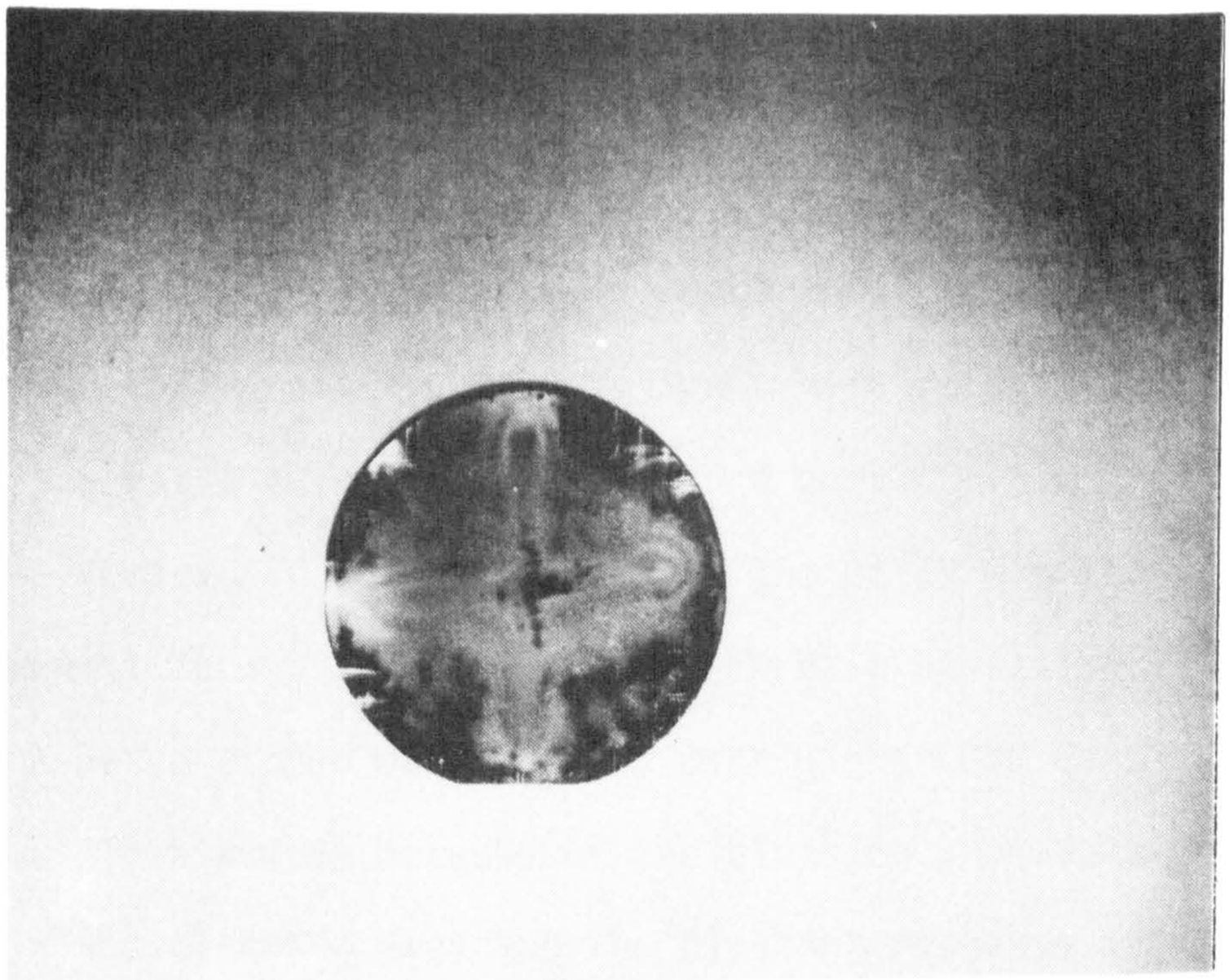


FIGURE 7.24 STAINLESS STEEL CONTAMINATION AT BACK SURFACE OF WAFER,FRONT SURFACE 1 MIN. SECCO ETCH

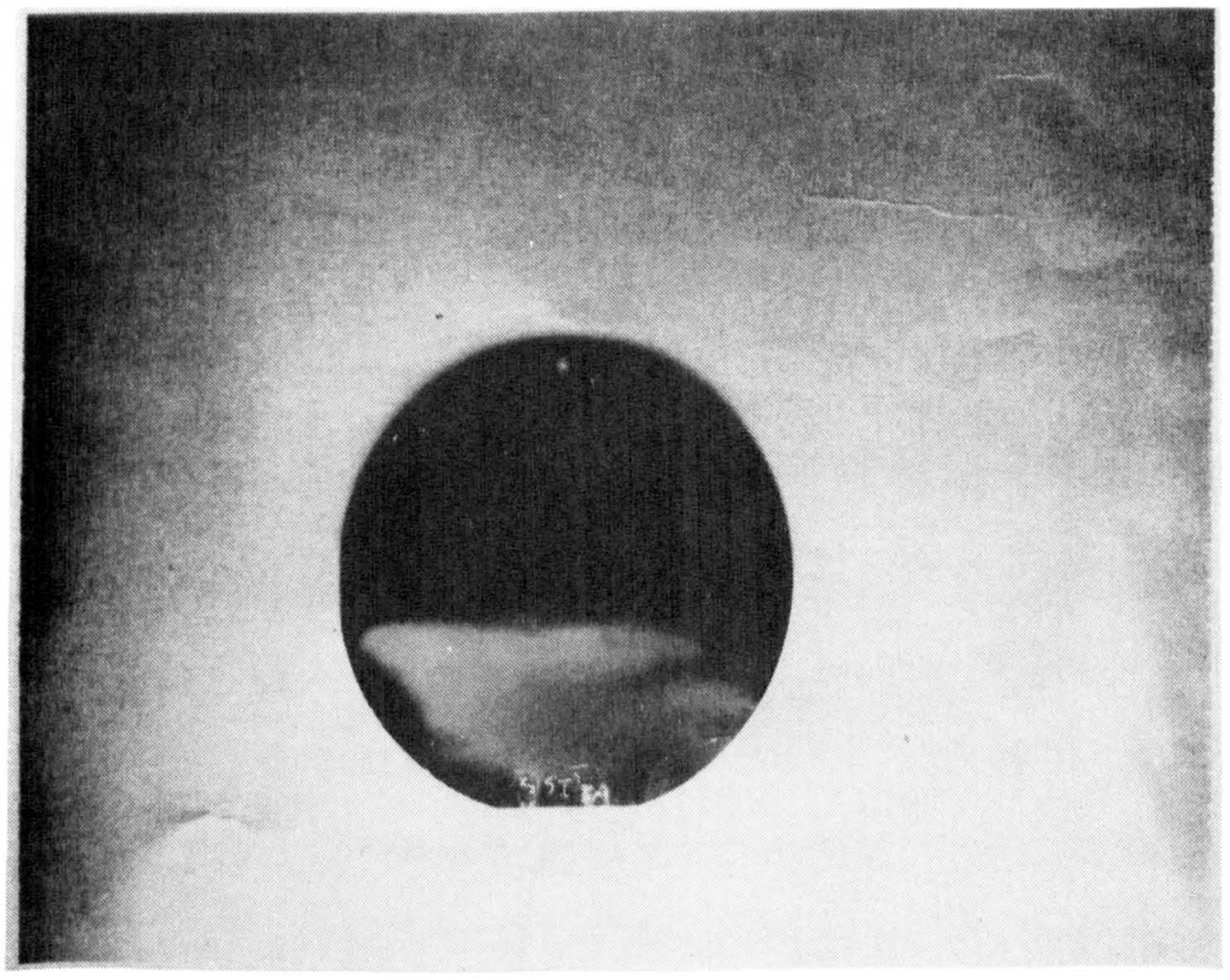


FIGURE 7.25 EFFECT OF INCORRECT CLEAN PROCEDURE PRIOR TO OXIDATION.
1 MIN. SECCO ETCH

an elapse time of one hour is possible between the two cleaning operations the first part of the batch is exposed to the furnace room ambient for a long time prior to the furnace operation. This procedure was found to increase OSF densities by up to two orders of magnitude on the first part of the batch relative to the second part. This difference could be removed if the first part of the batch was stored in high purity water until it was required for the furnace operation. Figure 7.25 shows a Secco etched wafer with a much higher OSF density over part of the wafer. This arises because of the cleaning procedure. The wafer was placed in the cleaning jigs and the cleaning reagents added one by one to the required mixture. The tide mark of OSFs shows where the first reagent was added. By preparing the cleaning solution and then adding the wafers this problem is overcome. The components of the clean, complex impurities in the individual reagents, avoid metallic impurities plating on the silicon. Obviously this factor is only of importance where the absolute quality of cleaning reagents cannot be guaranteed, and subsequent attempts to duplicate this result have met with varying success.

7.3.6. Elimination of Oxidation Induced Stacking Fault

(A) Pre Process Gettering

Various authors have suggested that gettering (i.e. gathering of unwanted impurities into benign regions) of OSF nuclei is possible. The most notable of these is a series of papers by Rozgonyi, Petroff and Read (31). These authors suggest that silicon wafers may be gettered prior to device processing by either a high concentration phosphorus diffusion into the back or silicon nitride deposition on the back of the wafer. This type of gettering has no effect on the device structure

and the wafers; thus there are no parameter changes to the transistor. A number of batches of device wafers were processed using these treatments (1 Ω per square phosphorus from 1100°C deposition, 2000Å Si_3N_4 deposited at 800°C.) No significant improvement in yield was observed because OSFs were still present. With a process such as Process III with eleven furnace operations the gettering effect with pre-process gettering is gradually reduced. That is, with each heat cycle the back surface gettering becomes less efficient and each process stage inevitably contributes to the total of unwanted impurities and hence possible OSF nucleation sites.

With the phosphorus back surface gettering OSF suppression was possible for five furnace cycles at 1100°C; the silicon nitride gettering was effective for three furnace cycles at 1100°C.

The phosphorus gettering operates by increasing the solubility of impurities in the misfit dislocations created by the high phosphorus concentration. The silicon nitride gettering results from thermal expansion mismatch stress set up in the wafer because of the nitride on the back. This results in a strain gradient across the thickness of the wafer and the OSF nuclei diffuse away from the front surface towards the back surface along this strain gradient.

A further technique investigated as a pre-processing treatment was the mechanical back lapping of wafers. This was done with a 13 μm lapping compound and 25 μm of silicon was removed. This gettering proved to be very efficient and increased yield was observed on some device wafers. However, it proved very difficult to adequately protect the front surface of the wafer during lapping and significant numbers of wafers were rejected because of front surface damage.

The Wacker Company of West Germany have introduced back damaged float zone material. This material is capable of withstanding six furnace cycles without growing OSFs. Device wafers processed with this material generally exhibit a higher than normal yield. However, on a significant number of occasions it has been shown that high densities of OSFs have occurred because the gettering mechanism has become inefficient as the process proceeded. A disadvantage of FZ material compared to CZ is an increased tendency to slip. Hu (32) has shown that oxygen in silicon pins dislocations; this has the effect of reducing slip. Hu's data suggests that an oxygen concentration of $\sim 6 \times 10^{17}$ at.cm^{-3} is necessary for any significant pinning and this value is nearly an order of magnitude larger than that typically found in FZ material and a factor of 2-3 less than that found in CZ material.

(B) <u>In Process Gettering</u>

The elimination of OSFs by pre-gettering device wafers prior to device processing was found to be ineffective. The alternative solution is to modify existing process stages such that they become gettering stages.

Investigations into thermal oxidation of silicon in ambients containing hydrogen chloride gas (33,34) have shown that OSF nucleation and growth can be eliminated.

The mechanism by which HCl affects OSF growth and nucleation is not clear. Hu (27) suggests that OSFs grow because there is an incompleteness in the silicon oxidation process during thermal oxidation. This incompleteness in oxidation leaves a small quantity of silicon atoms as excess interstitials at the silicon-silicon dioxide interface. The excess interstitials are not in equilibrium with the silicon lattice;

the growth of an extrinsic stacking fault removes some of the excess interstitials, helping to restore equilibrium. The oxidation of silicon is thought to occur by the diffusion of oxygen through the growing oxide layer to the oxide silicon boundary. High concentrations of HCl are known to result in silicon etching (Figure 7.26). If silicon atoms were removed from the oxide silicon boundary by low concentrations of HCl then the excess of interstitials in the silicon surface would be decreased. Further, as silicon removed by the HCl must be transported through the growing oxide there is the possibility of silicon oxidation occurring in the growing oxide not just at the oxide silicon interface. This would be manifested as a slight increase in the oxide growth rate. Experimentally silicon oxidises faster in O_2/HCl ambients than in O_2 alone. This is attributed to both enhanced Si-Si bond breaking due to etching by HCl and to water formation (36). Thus the removal of silicon from the oxide silicon interface by chlorine species is the likely mechanism for OSF growth suppression in dry oxidation ambients containing HCl.

HCl oxidations were investigated using trichloroethane 111 ($C_2H_3Cl_3$) known as C_{33}. This material produces 3 volumes of HCl for each volume of vapour. The reported HCl oxidation treatments have all been related to dry oxidations. These are suitable for gate oxidations in MOS processes. Bipolar processes require thick field oxidations or diffusion re-oxidations ($\sim$ .3 μm to .5 μm thick). This requirement and the limitations imposed by diffusion means that bipolar processes require wet oxidations. The first and second oxidation are the field type oxidations in Process III. HCl gettering oxidations are ideal at these stages as nucleation of OSFs due to swirl defects can be eliminated. The technique adopted is to first grow a dry HCl gettered oxide and then change over to steam to thicken the oxide.

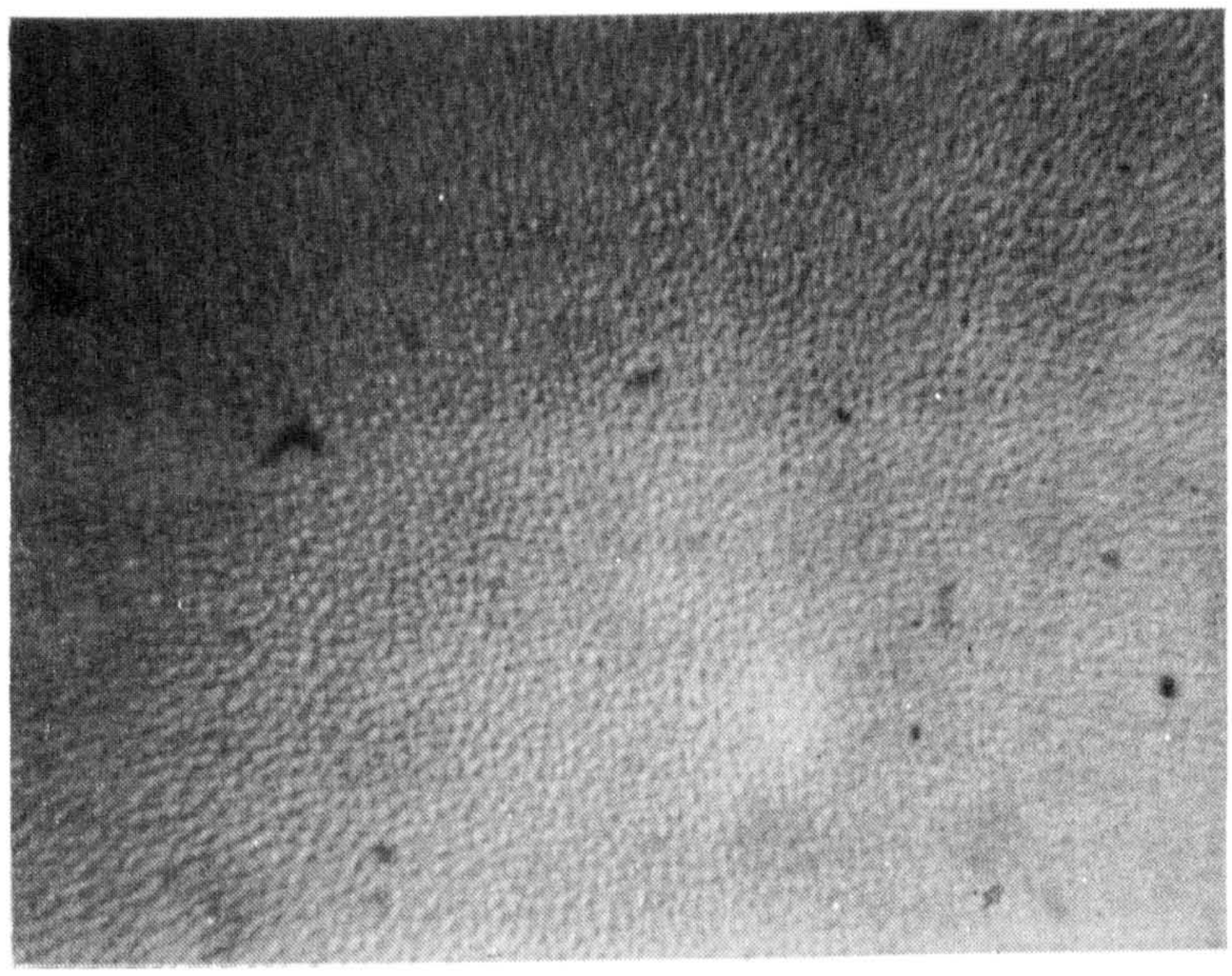


FIGURE 7.2 6. HCl ETCHING OF SILICON

6% HCl in O_2 at 1100°C (X600)

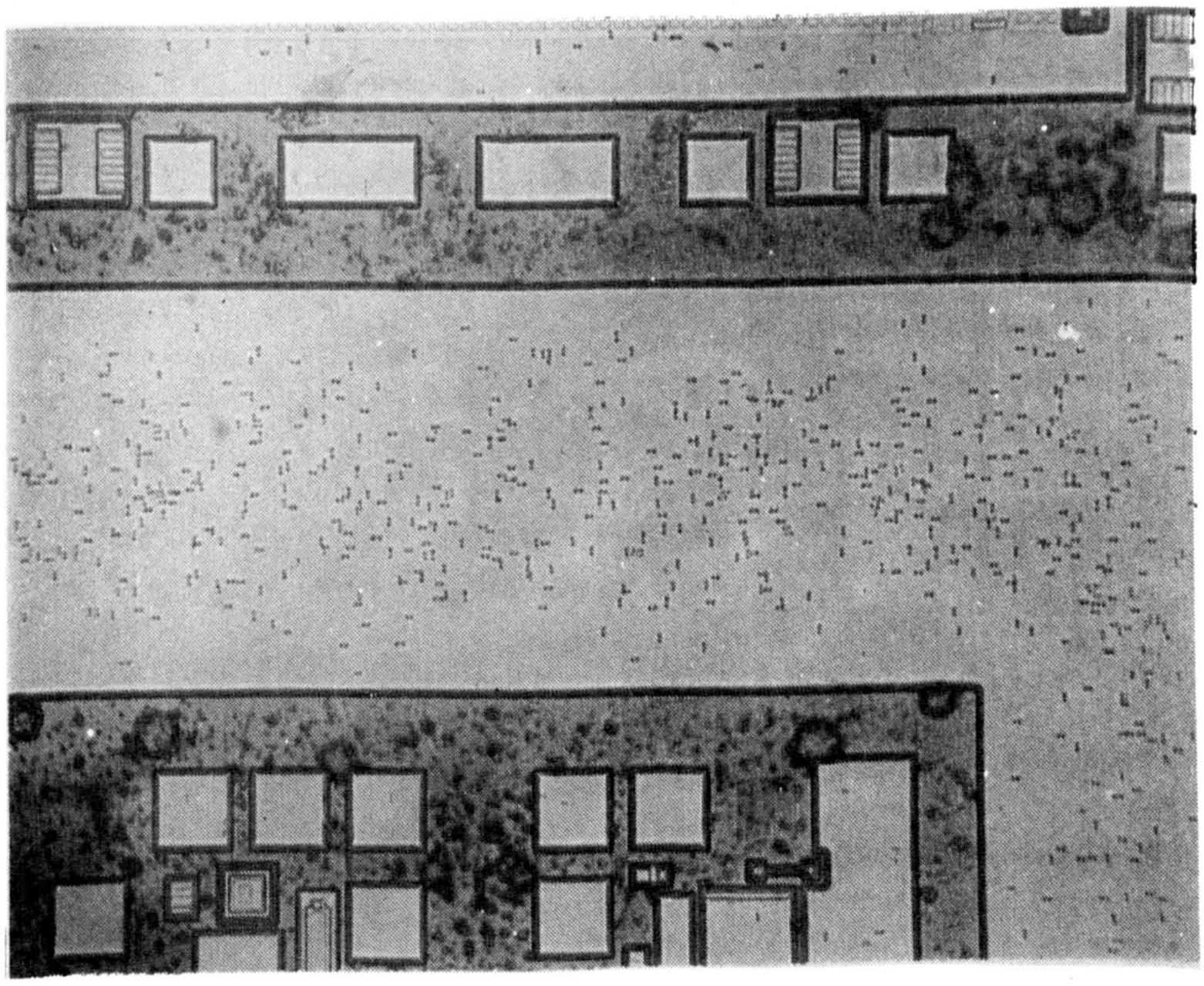


FIGURE 7.2 7 ISOLATION (BORON) DIFFUSION GETTERING

1 min. Secco Etch (X45)

The first and second oxide growth temperature is 1100°C. HCl gettering treatments were investigated at this temperature and at 1000°C and 1150°C. The HCl concentration and the dry oxidation period were varied. At 1000°C it appeared that HCl concentrations in excess of 6% were required to minimise OSF growth; unfortunately results were varied and inconsistent. HCl concentrations of 2% at 1150°C suppressed OSF growth. As slip is less at 1100°C than at 1150°C a thorough investigation of the 1100°C process was performed. At 1100°C OSF suppression is achieved if the wafers are oxidised for 20 minutes in dry oxygen with 4% HCl. At concentrations higher than 4% there is a danger of etching the silicon surface. Figure 7.26 shows a wafer surface after 20 minutes dry oxygen with 6% HCl. There is extensive etching of the wafer surface. The schedule adopted is as follows:

20 minutes dry O_2 4% HCl)
) in the same furnace at 1100°C
50 minutes steam)

This schedule grows .54 μm of oxide.

As the misfit ratio, i.e. the ratio of the Pauling covalent radius of solute to silicon atoms, of substitutional boron is smaller than that of phosphorus (.746 compared to .932) a given atomic fraction of boron in silicon will produce a larger strain than phosphorus (35). A high boron concentration will generate misfit dislocations which are similar to the gettering sites in phosphorus high concentration diffusions. The isolation diffusion had been shown to preferentially nucleate OSF, the initial Process III isolation does not getter. As a gettering experiment the deposition time at the initial temperature (1000°C 30 Ω/sq.) was increased from 30 minutes to 2 hours with a 50% reduction in resistivity; no gettering was observed. Using 1050°C and a 1 hour deposition

(ρ_s, 8 Ω/sq.), however, very effective gettering was observed (Figure 7.27). The gettering range of the isolation diffusion is approximately 150 μm in this case. Thus, by depositing into the back of the wafer, front surface gettering is not observed as the thickness of the wafer is 450 μm. However, by slightly improving the treatment conditions front surface gettering and OSF suppression was achieved with the isolation diffusion (Figure 7.28). (The drive-in time was modified to achieve standard junction depths).

The treatments of Rozgonyi (31) show that phosphorus diffusion into the back of wafers is a very effective getter for OSF nucleation sites. The Process III deep N^+ diffusion is a high concentration phosphorus diffusion. However, with the initial Process III schedule no gettering is observed. The temperature of the deposition was increased from 875^oC to 1050^oC. At this temperature the phosphorus deep N^+ becomes a very effective getter. A further improvement was obtained by increasing the temperature of deposition to 1100^oC. Figure 7.28 shows a Secco etched Monsanto CZ wafer on which a standard 0.5 μm thermal oxide had been grown. Selected areas of the back of the wafer received the modified isolation and deep N^+ diffusions. The Figure shows clearly the quadrant of the wafer which received no gettering. The OSF density in this region is $\sim 10^4$ cm^{-2} and near zero in either of the gettered parts. The drive-in schedules of the deep N^+ and isolation diffusion were also modified to grow the minimum OSF length possible. This was achieved by changing the furnace ambient to nitrogen after the required re-oxidation thickness had been achieved.

As further evidence of the effectiveness of the 1100^oC deposition phosphorus deep N^+ diffusion, Figure 7.29(a) shows a Secco etched wafer after isolation diffusion which had been inadvertently contaminated. Four other wafers from this batch gave similar results. The remaining

UNGETTERED

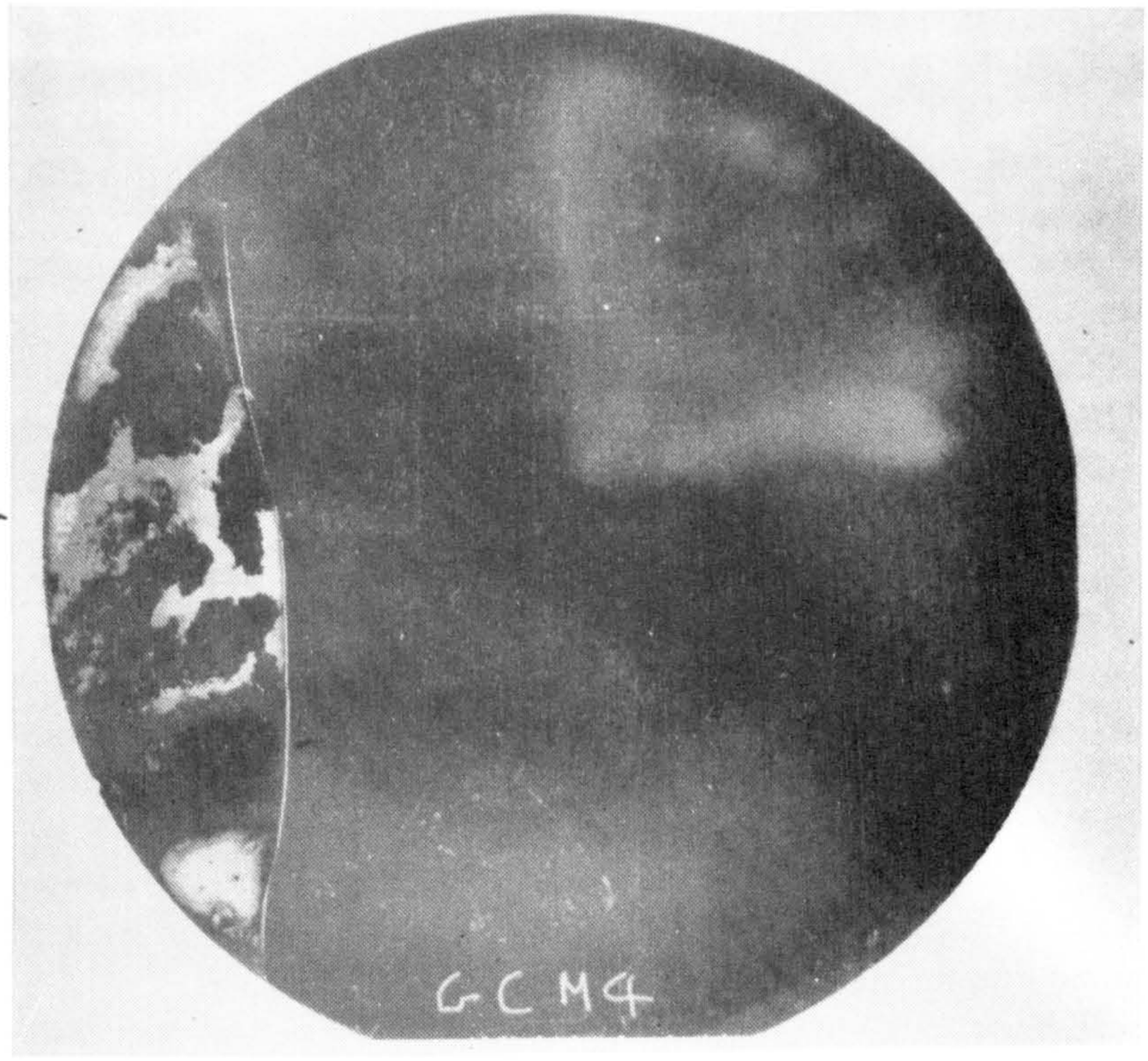
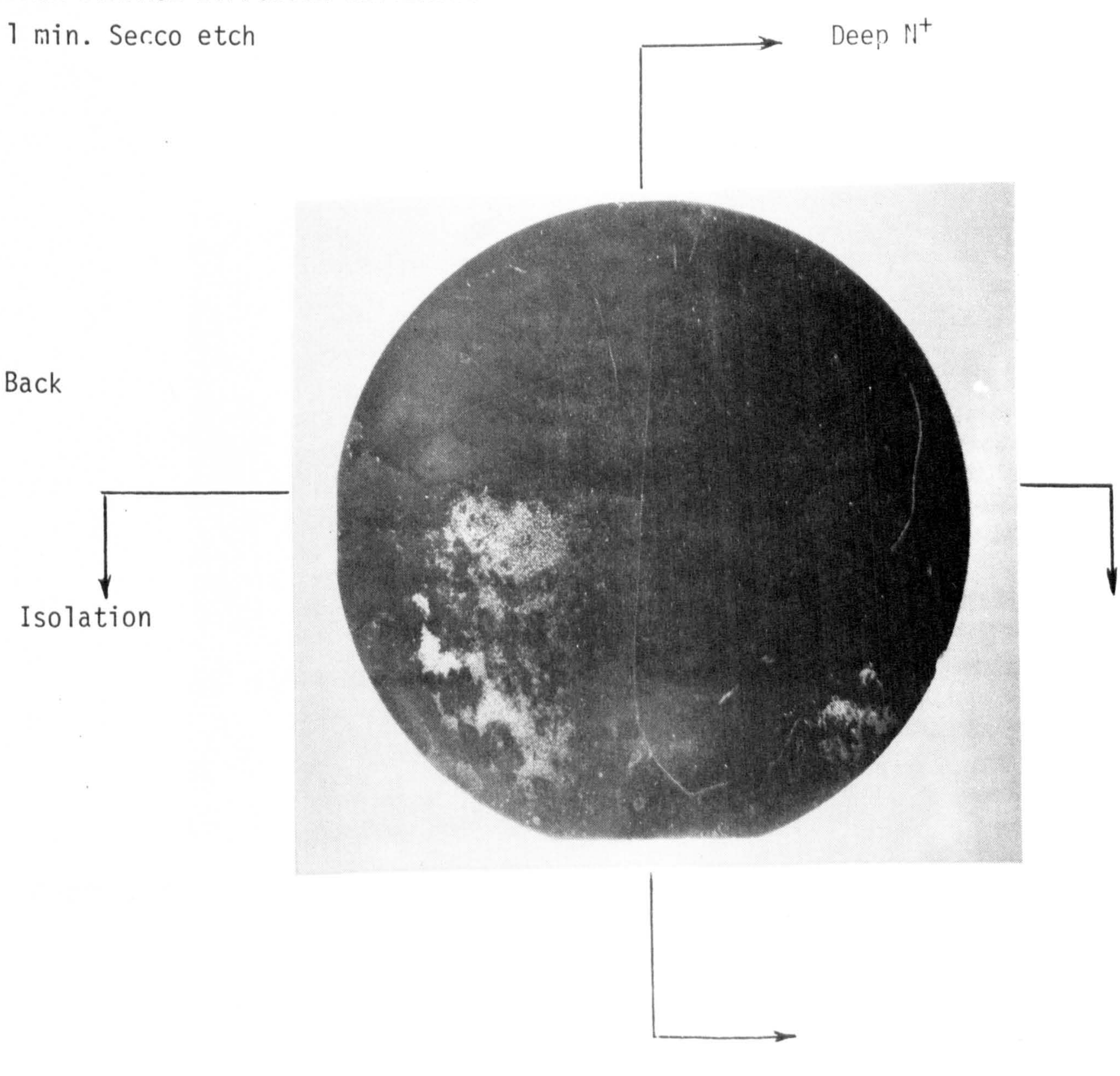


FIGURE 7.2 8

BACK SURFACE DIFFUSION GETTERING



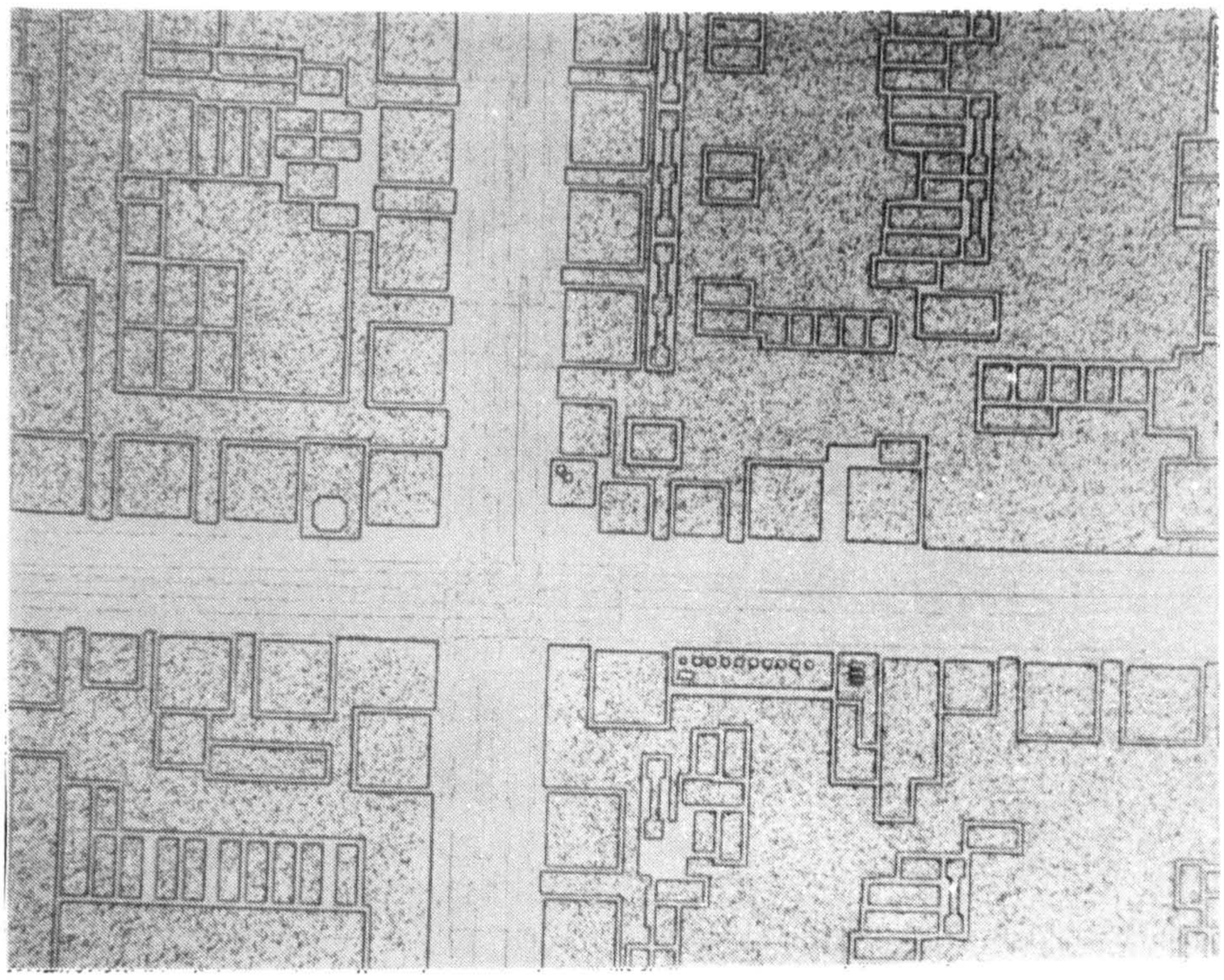


FIGURE 7.29(a) WAFER CONTAMINATED AT ISOLATION DIFFUSION
1 min. Secco Etch (X45)

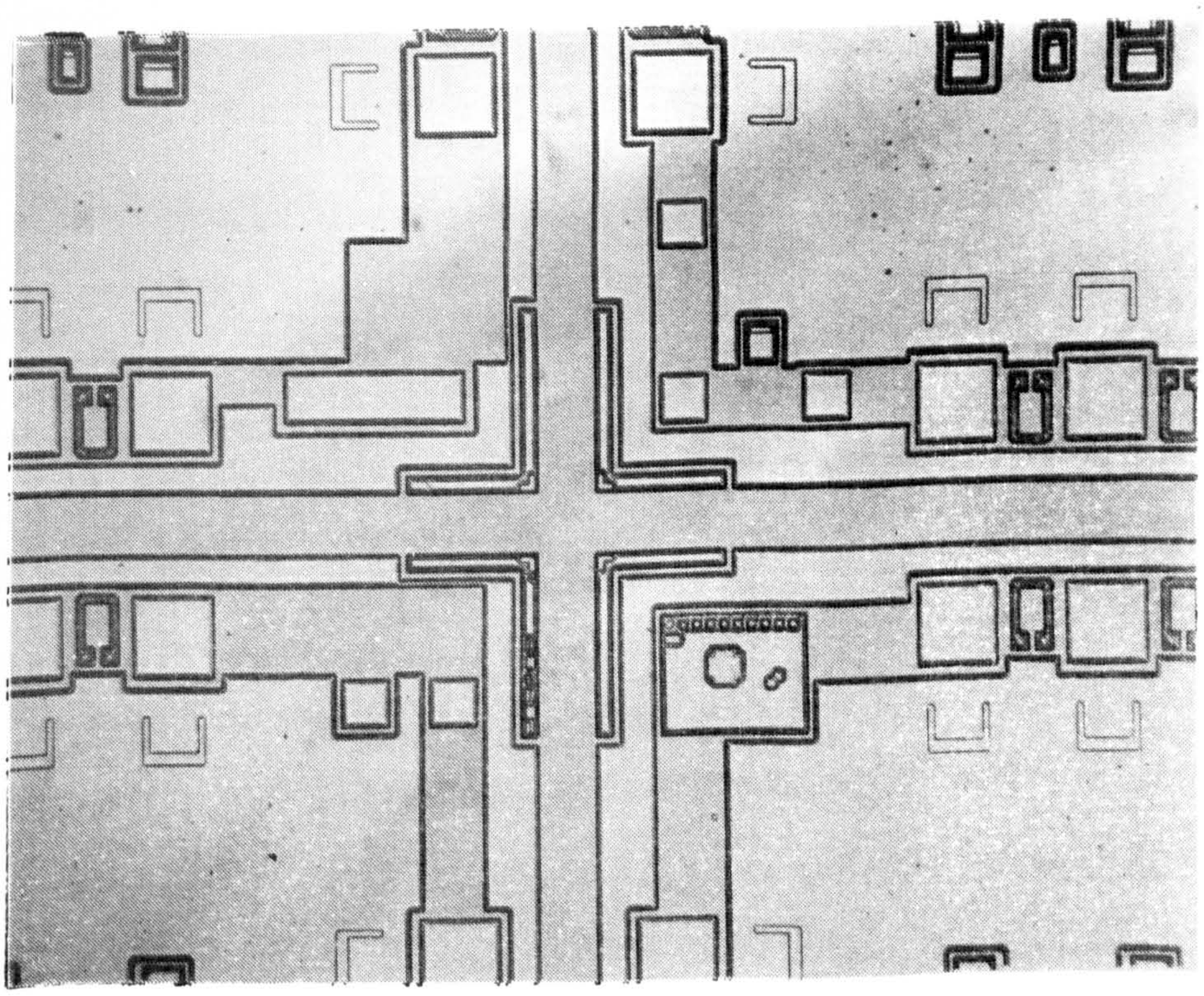


FIGURE 7.29(b) WAFER CONTAMINATED AT ISOLATION DIFFUSION AFTER
COLLECTOR GETTERING TREATMENT. 1 min. Secco Etch (X45)

wafers were processed through the gettering collector process. Figure 7.29(b) shows a typical result after Secco etch viz. total elimination of defects. The defects shown in Figure 7.29(a) were investigated by TEM (Figure 7.30). The defects are short highly decorated OSFs.

The gettering collector is compatible with Process III. The sheet resistivity is reduced from the previous standard of 4 Ω/sq. to 2 Ω/sq; junction depths are similar.

7.4. COMPARISON WITH RESULTS FROM OTHER PROCESSES

In order to establish if the results obtained on Process III were similar to those obtained on other bipolar processes, a number of I^2L wafers from Plessey consumer Process (D) were examined as were those from another manufacturer who uses a shallow diffused (base $x_j \sim 1$ μm) Schottky TTL process for I^2L. It had been established that all variants of Process III suffered from the same yield mechanisms. Figure 7.31 shows a Process D transistor with an epitaxial stacking fault in the shallow N^+. This transistor is not a failure. In general no collector-emitter pipes were observed on Process D either from slip dislocations or stacking faults. This process is very deep, having a collector-base junction depth 2.5 μm and base width .5 μm compared to .4 μm and .25 μm respectively for Process III. It is thought that this increase in depth and base width is responsible for the high process yield. This is in spite of the fact that no effective gettering stages are incorporated into Process ID.

The Schottky process showed no evidence of pipes. The base width of these transistors was of the order .3 μm. This is similar to Process III, as is the base junction depth. Examination of the process

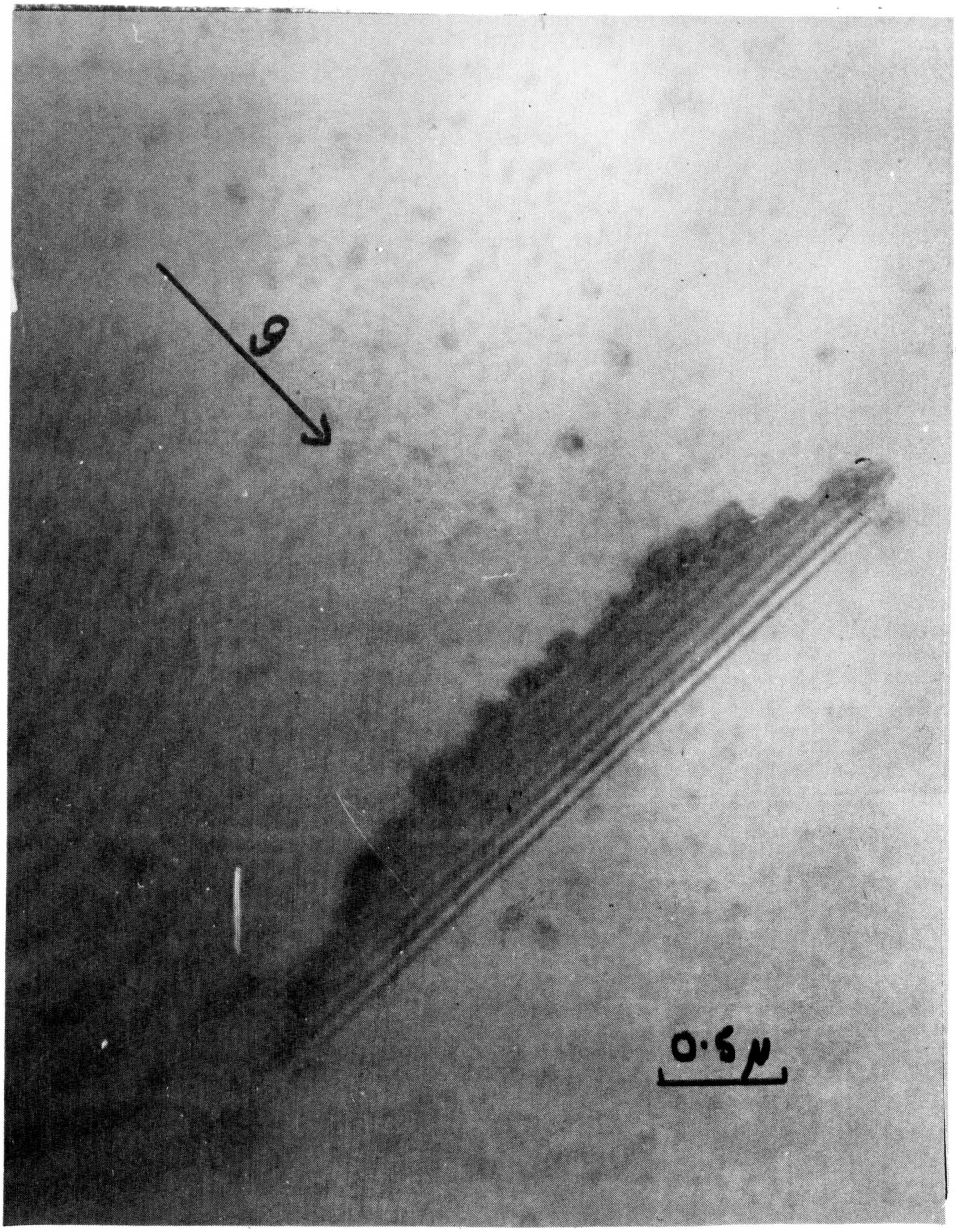


FIGURE 7.30 SHORT OSFs RESULTING FROM WAFER CONTAMINATION

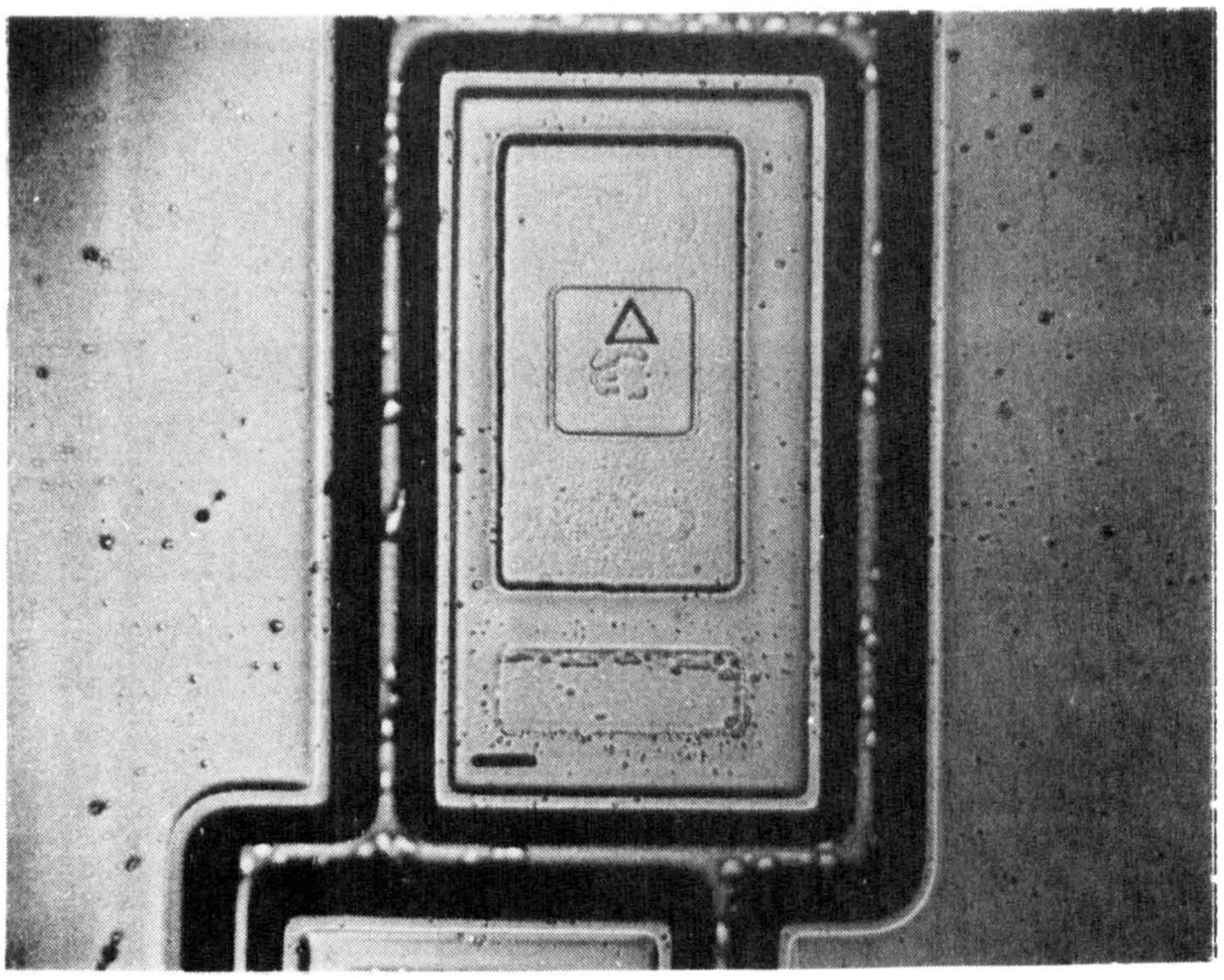


FIGURE 7.31 PROCESS D GOOD TRANSISTOR

2 min. Secco Etch (X500)

schedules showed that the isolation and collector diffusions were ideal gettering treatments based on the evidence obtained on this study. The wafers had been very carefully processed and showed minimal slip. Devices in slip regions showed poorer breakdown but no pipes.

Both the previously described processes use (111) orientated silicon as opposed to Process III which uses (100). Hu (27) shows that silicon orientation is very important for OSF growth and that (111) orientation produces low OSF densities. OSF densities observed are indeed much less than that on Process III. These and other crystal defects do not appear to relate to device failure. However, because the results on both these processes are similar the reason for the similarity is not necessarily the orientation. The consumer process has a deep wide base emitter structure and the Schottky TTL process is well gettered.

7.5. CONCLUSION

The purpose of this chapter has been to describe the practical problems encountered in the development of the state of the art high performance bipolar LSI technology. At the time of writing the Plessey Company is capable of producing bipolar LSI devices of considerable complexity with economic yields. However, the semiconductor industry is such that the circuits required for production in subsequent years will always be larger and more complex than those currently in production. This means that the yield improvement exercise is a continuous process, with increased attention to the small details of processing as time elapses.

The work described here is that which changed Process III from being medium scale integration to an LSI process. A factor of at least

ten improvement in yield was obtained in the I^2L circuit WM7 shown in Figure 1.10. This result showed that I^2L on Process III is a viable technique for the implementation of digital LSI circuits.

CONCLUSION

It has been demonstrated in this thesis that the relatively simple expressions derived predict fairly accurately the physical processes operative in the I^2L gate. Using these expressions it has been shown how the gain of transistors operating in the I^2L mode depends upon the ratio of collector to base area, resistive debiassing and high level injection. The latter phenomena has a profound effect on the device performance. The treatment for the collector current of the lateral pnp shows that it is dependent on the two dimensional nature of the base region. The d.c. theory is adequate to predict the performance of I^2L on a number of processes.

The a.c. performance has also been modelled and shows that the operation falls into two fairly distinct regimes, described as the extrinsic and intrinsic regions.

The major parameters controlling delay in the extrinsic delay regime are depletion capacitance and the common base current gain of the injector pnp transistor. In the intrinsic delay regime the delay is shown to be dependent on minority carrier charge storage, collector current and resistive debiassing. The different effects, of changing the gain of the I^2L gate by modifying either base or collector current, on intrinsic delay, is also determined. These theoretical predictions are confirmed by experimental observation.

In I^2L circuits an unusually high percentage of the chip

area is taken up by active base region. A major yield limitation is therefore the 'collector emitter' pipe. A large amount of experimental work established that crystal slip and oxidation induced stacking faults are the major cause of 'pipes' but they can be virtually eliminated if the correct procedures in oxidation and diffusion are adopted.

At the inception of I^2L itwas felt that it offered a real bipolar alternative to MOS for large scale integration of logic. In the six years since this event, I^2L has not in practice been used to displace MOS as a logic technique. Rather, it has been used in a different role, viz: the implementation of combined functions, for example, logic with other types of circuitry, such as linear or high power drivers. This type of function is ideally suited to I^2L because peripheral conventional bipolar transistors are well suited to both linear and high current drive applications.

To obtain best logic performance of I^2L, specific processes capable of exploiting the super integrated nature of the gate have been developed, at the expense of good peripheral transistor performance. These approaches have included attempts at reducing the charge storage in the gate by adding Schottky barrier diodes as anti-saturation clamps, or in series with the gate to limit the logic swing.

Appendix 8 describes one of these specific I^2L logic processes which demonstrates the full potential of the I^2L gate as a logic element.

APPENDIX 1

PROCESS III

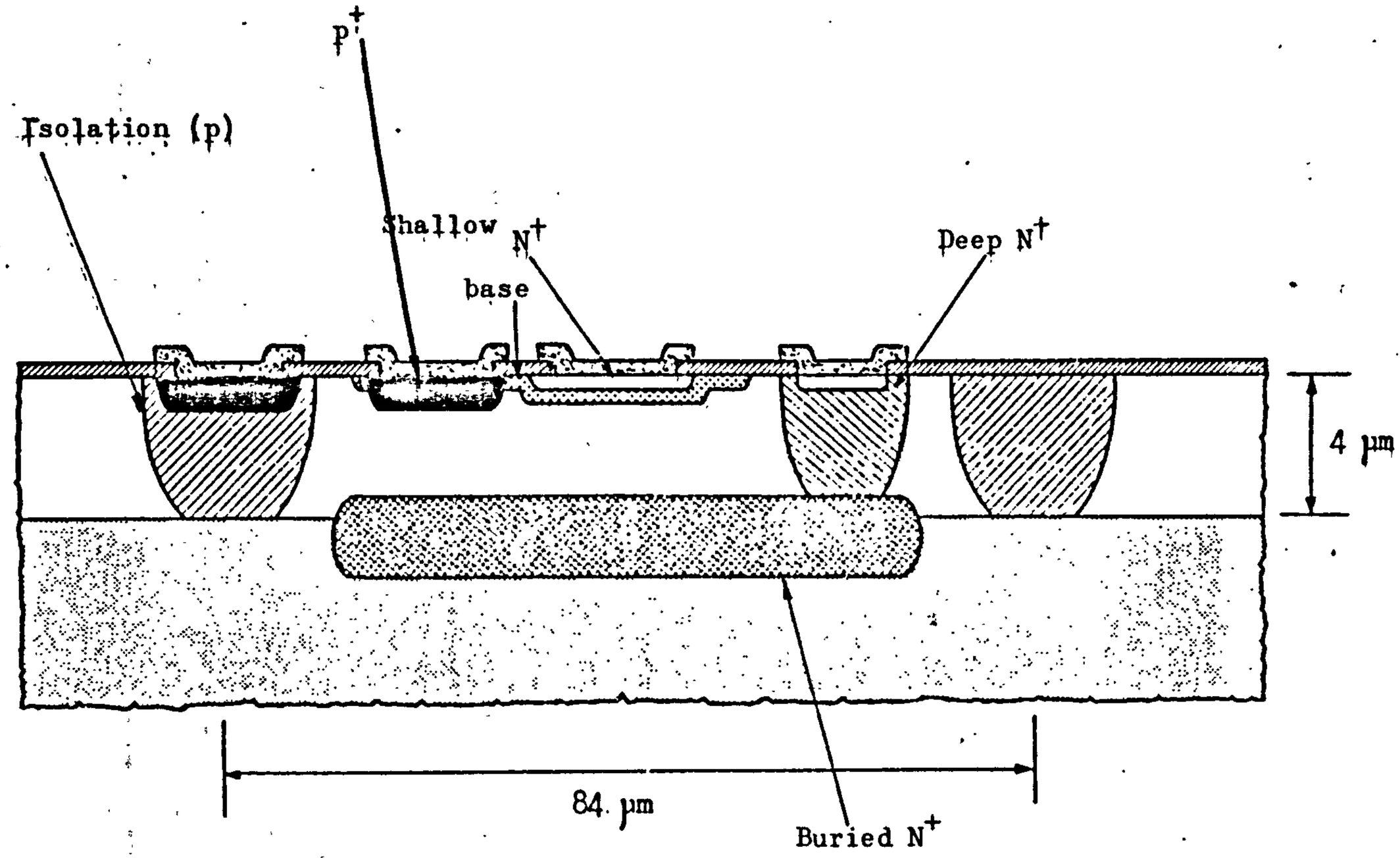
Process III is a shallow diffused high speed bipolar integrated circuit process. The process was originally developed in the late 1960's and early 70's for the manufacture of very high speed emitter coupled logic circuits. These functions require nanosecond or sub-nanosecond switching delays, are low in complexity and have a significant power consumption per logic function. The process has titanium aluminium metallisation, and an additional diffusion (p^+ resistor) included for low value resistors. This diffusion is used also to obtain low contact resistance to all p-type regions. The process was not designed for LSI.

Figure A1.1 shows a cross section of the basic npn transistor. The layout of a double base contact device is shown in Figure A1.2.

TABLE A1 1

Substrate	5 Ω cm P	
Buried N^+	12 Ω/□ (arsenic)	
Epi	4.2 um 2 Ωcm N	(phosphorus)
Isolation	60 Ω / □ x_j 6.5 μm	(boron)
Deep N^+(Collector)	3.5 Ω / □ x_j 4.5 μm	(phosphorus)
P^+ resistor	60 Ω / □ x_j 0.8 μm	(boron)
Base	450 Ω / □ x_j 0.4 μm run-on·65 μm	(boron)
Shallow N^+ (emitter)	25 Ω / □ x_j 0.4 μm	(phosphorus)

The lateral pnp transistor uses the P^+ resistor diffusion for the emitter and collector. The P^+ resistor diffusion is used because its high doping improves emitter injection efficiency.



Structure of npn transistor (recut emitter)

FIGURE A.1.1.

Process III Planar npn transistor (Computer graphics plot)

RB20

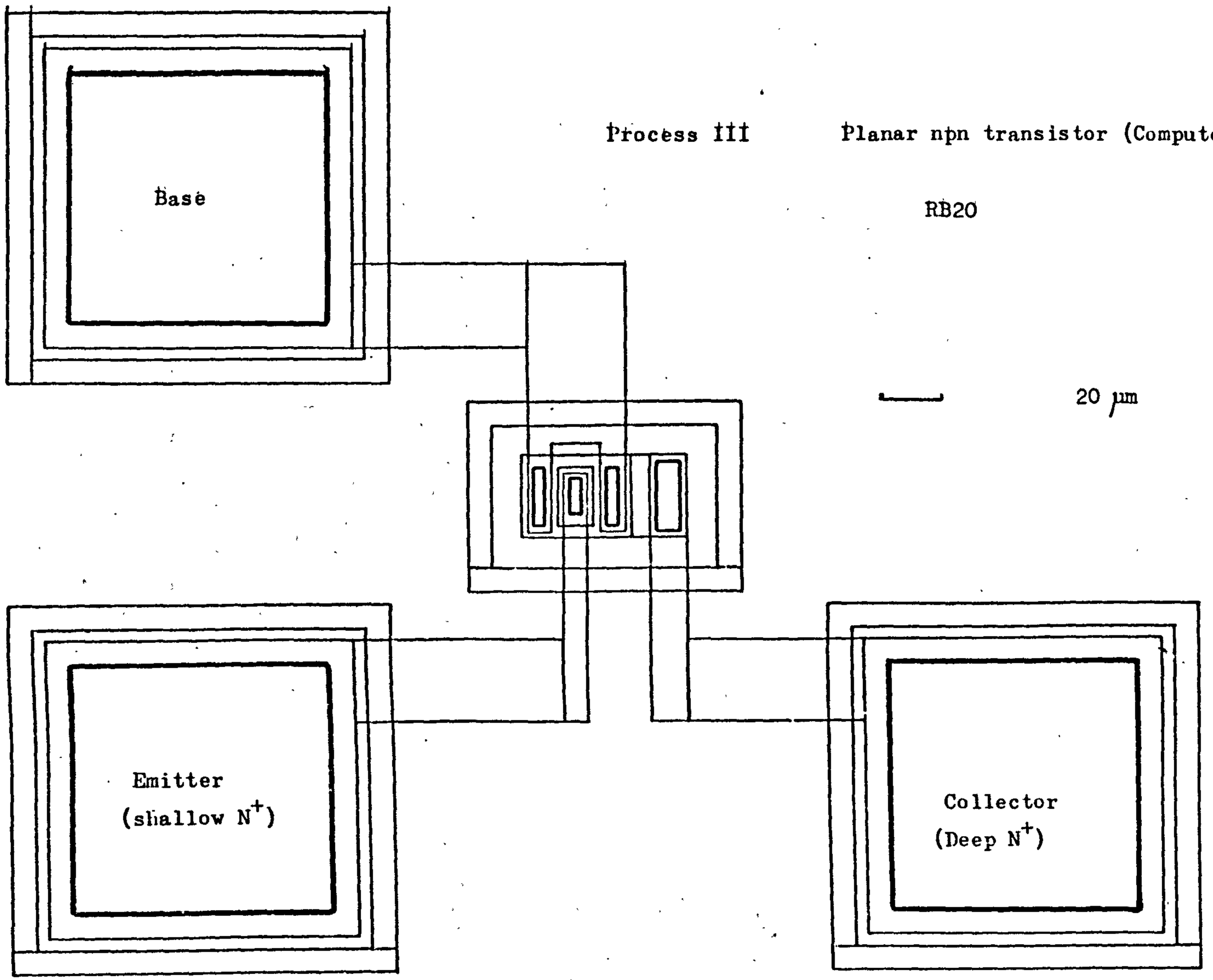
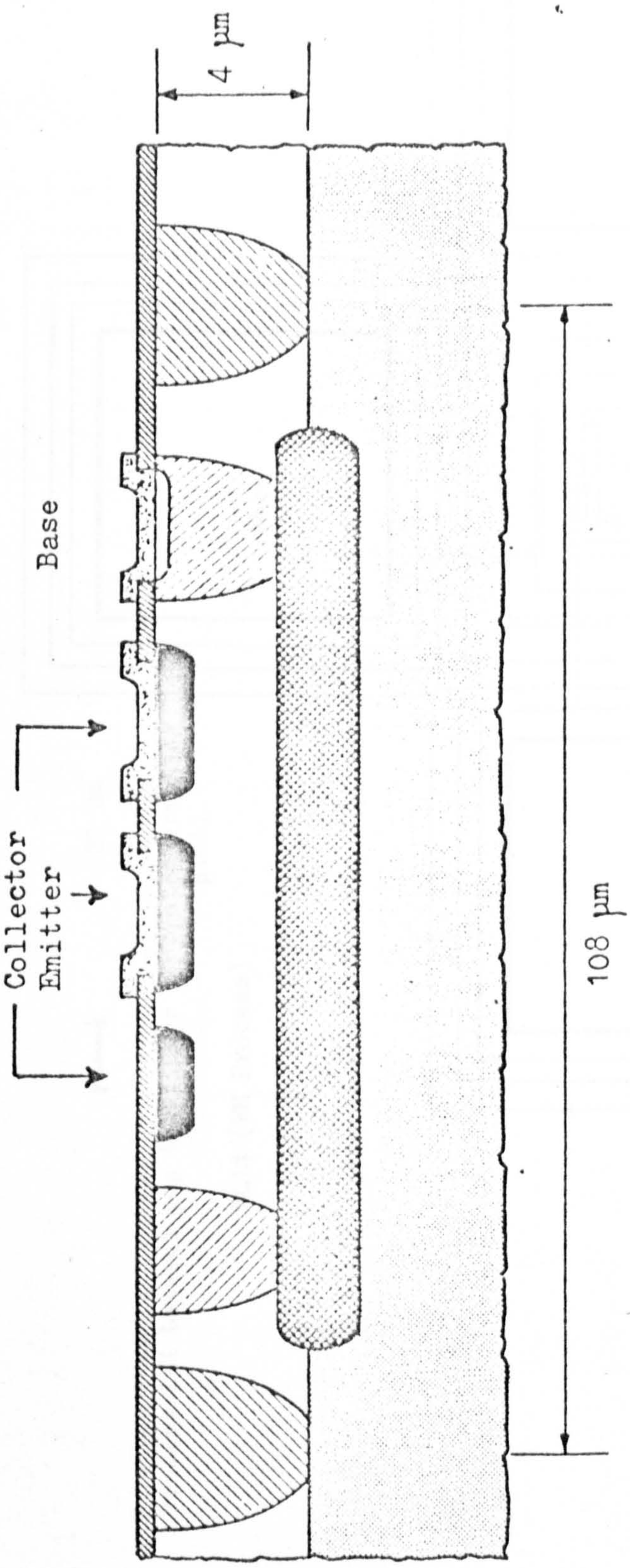


FIGURE A1.2.



Lateral pnp transistor

FIGURE A1.3.

20 um

Process III Lateral pnp transistor (Computer graphics plot)

RL14 (WM Process)

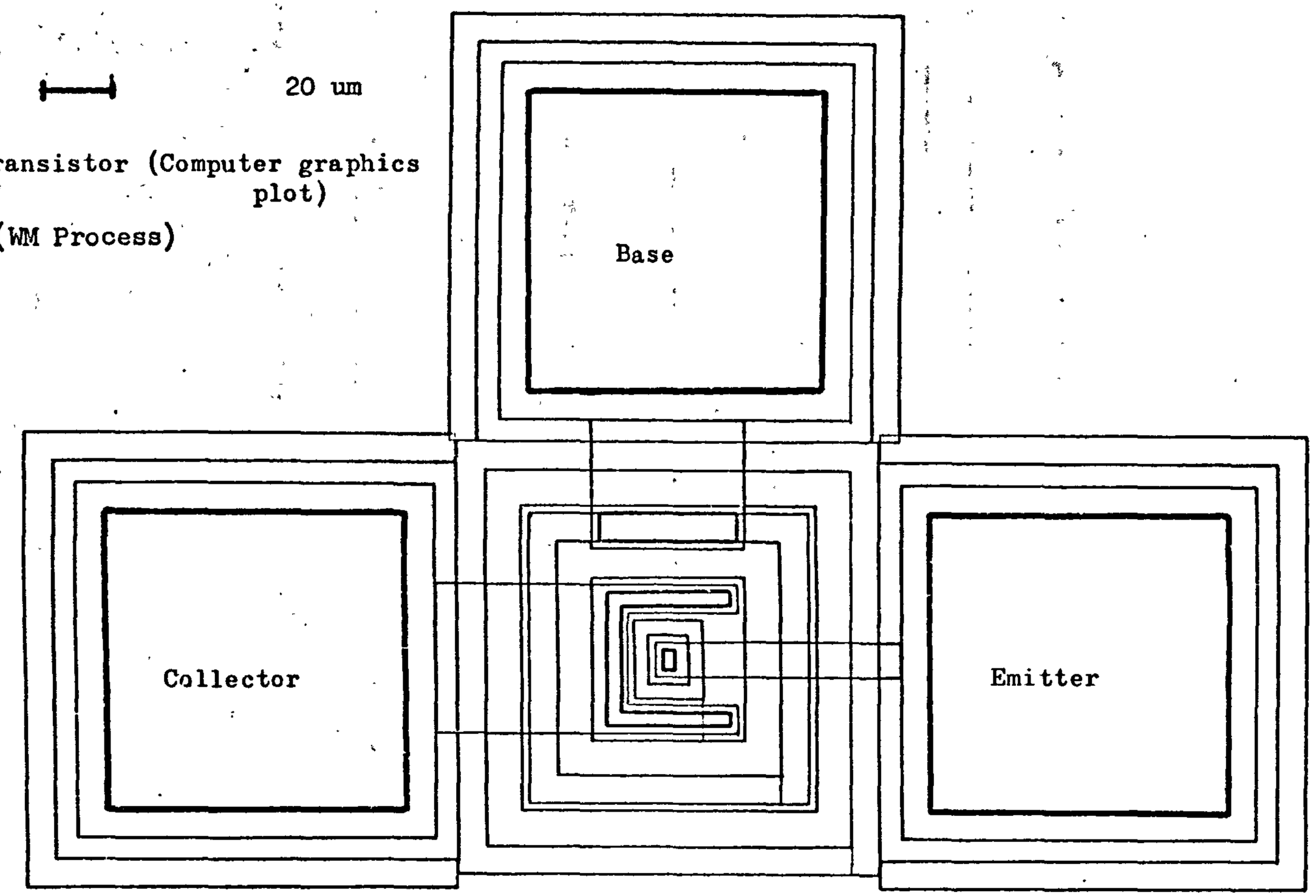


FIGURE A1.4.

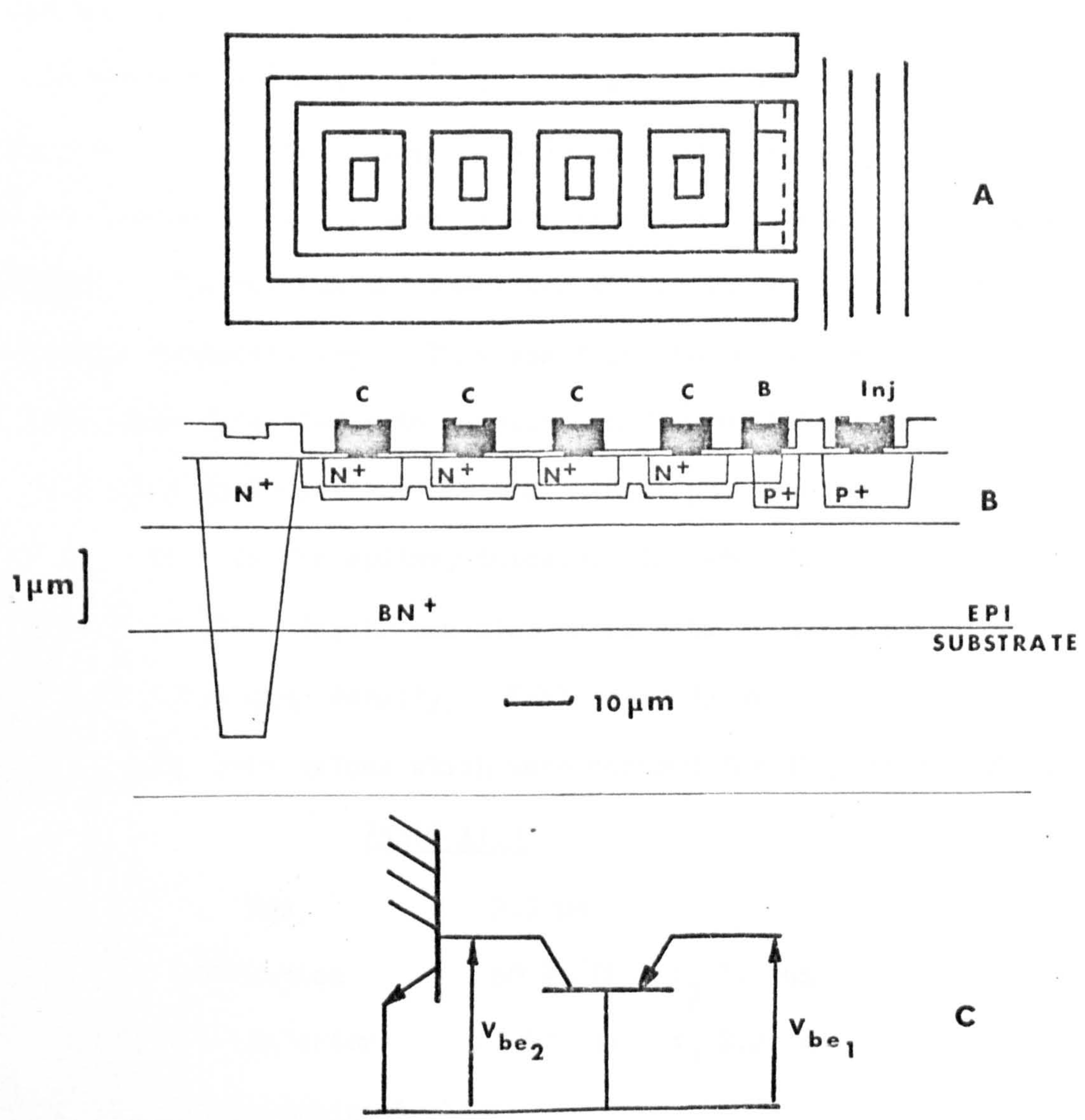

BASIC BIPOLAR PROCESS III I²L GATE
A
C C C C B Inj
N+ N+ N+ N+ N+ P+ P+
B
1µm
BN+
EPI
SUBSTRATE
10µm
C
Vbe2
Vbe1
POWER x DELAY ~ Vbe1 Vbe2 C / a

FIGURE A1.5.

Figures A1.3 and A1.4 show cross-section and layout of the lateral pnp transistor.

Table A1.1 details the major characteristics of regions of the Process III transistor.

In order to produce an I^2L process with a power delay product of ~ 1 pJ and minimum gate delay of the order of 25nS for a four collector gate it was necessary to reduce the epitaxial thickness. The minimum thickness was set by the requirement for TTL voltage compatibility. This was found to be 2.2 um. The basic four collector gate is shown in Figure A1.5. The collector size is 12 x 14 um and the lateral pnp injector base width is 4 um. As the epitaxy thickness is reduced, isolation and deep n^+ junction depths can also be reduced with a subsequent improvement in packing density. Table A1.2 details the parameters and their values which were changed for I^2L optimisation.

TABLE A1.2

Epi	2.2 μm	
Isolation	60 Ω/□	x_j 3.2 μm
Deep N^+ (collector)	3.5Ω/□	x_j 2.2 μm

Depletion region recombination

In order to investigate low current gain mechanisms in Process III transistors a series of V_{be}; I_C I_B measurements were made on devices of various geometries. The measurements were carried out on downward operated npn transistors and comparisons were made between devices on the same silicon chip. All measurements are with $V_{CB} = 0$ to eliminate collector-base leakage from the measurements.

PROCESS III DOWNWARD TRANSISTOR

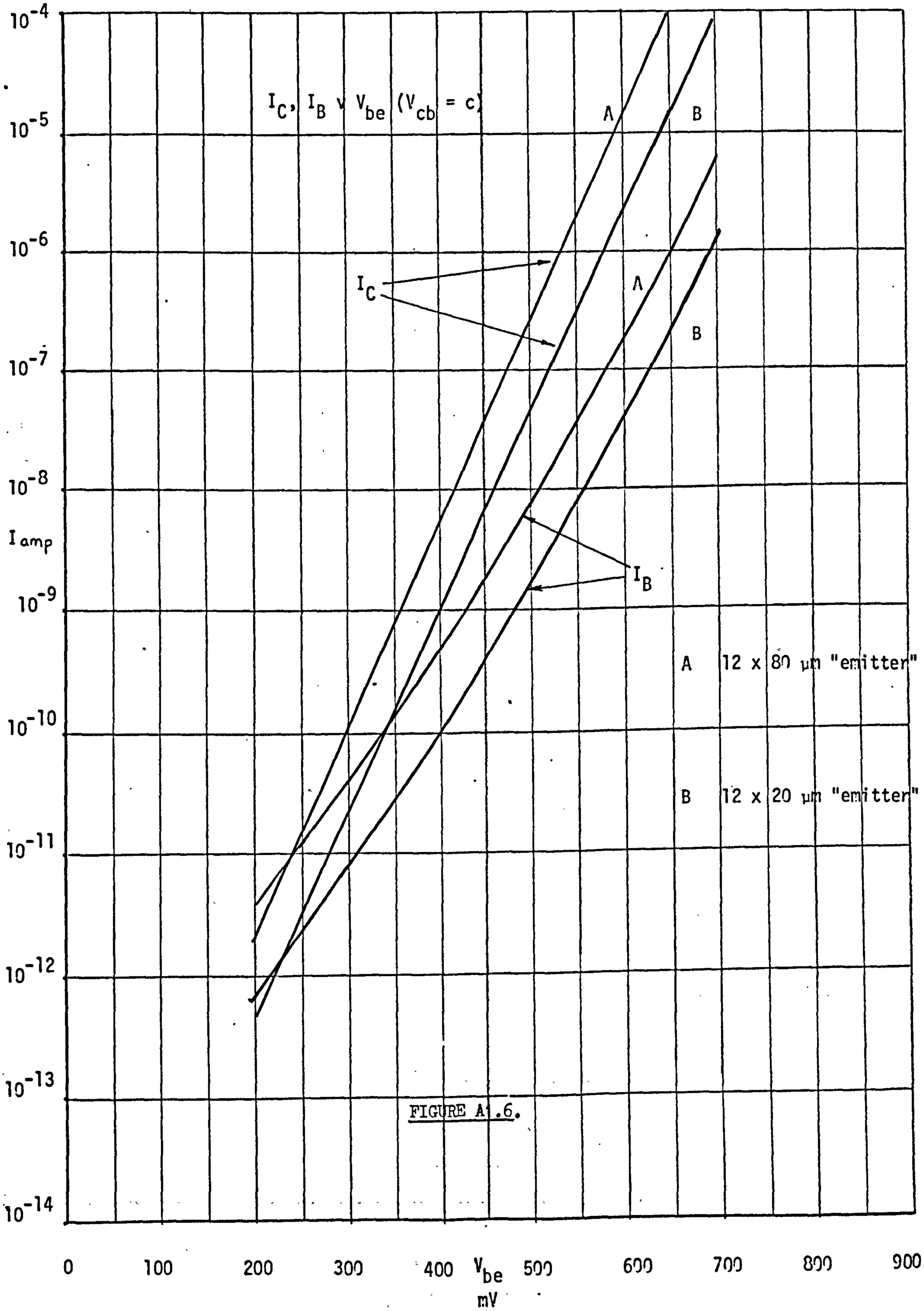


FIGURE A1.6.

PROCESS III DOWNWARD TRANSISTOR

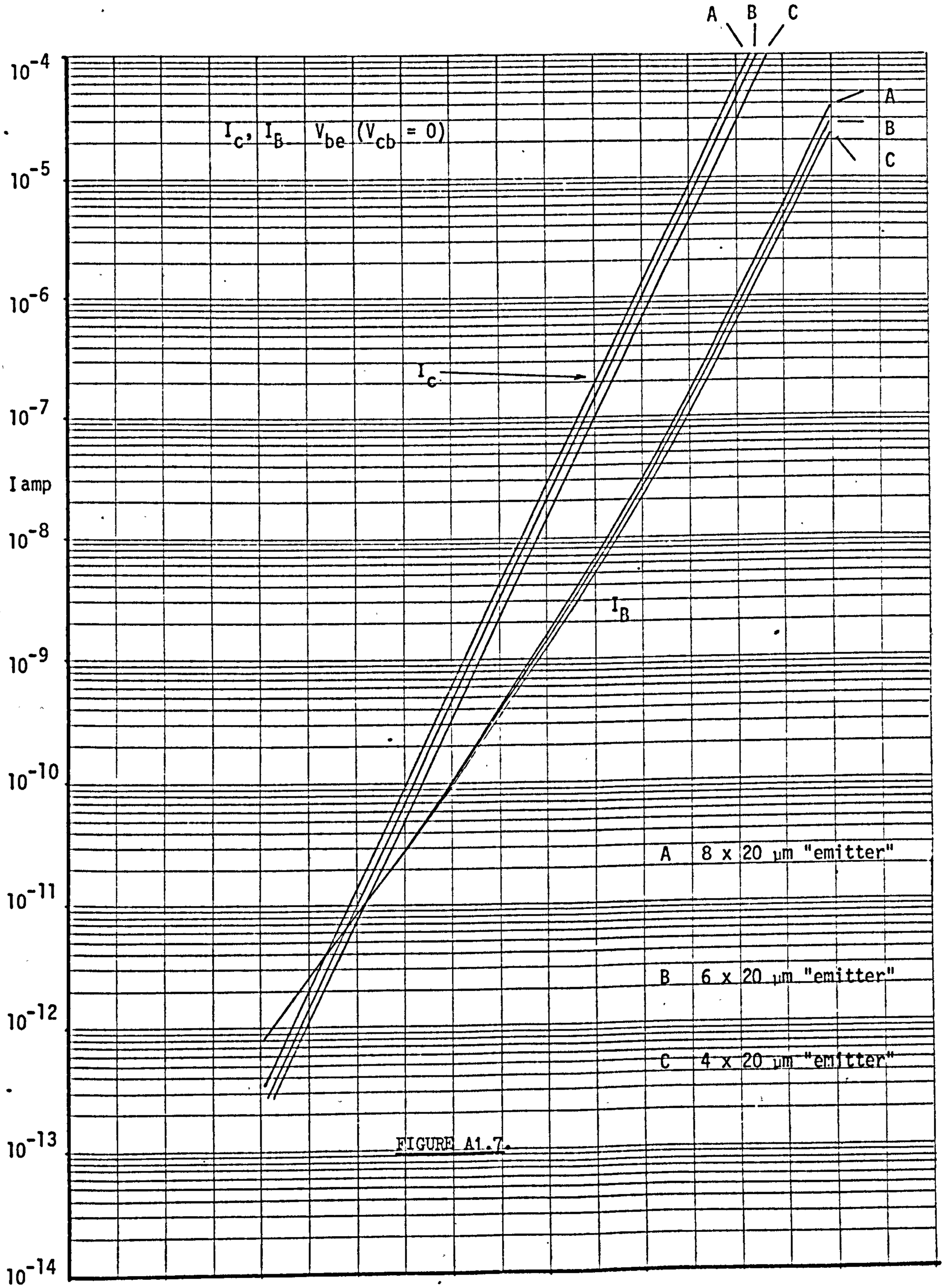


FIGURE A1.7.

Figure A1.6 shows a comparison of V_{be}, I_C, I_B characteristics for transistors with 12 μm x 20 μm and 12 μm x 80 μm emitters. Note the distinct two regions of the base current characteristic. I_B is of the form

$$I_B = I_o \exp {}^{qV}/_{nKT}$$

where n is varying from 2 to 1. The n = 2 characteristic results from depletion region recombination [1].

Figure A1.7 shows a comparison of V_{be}, I_C, I_B characteristics of transistors with 4 x 20, 6 x 20 and 8 x 20 micron emitters. In these devices the emitter area is varied by changing stripe width only such that the emitter perimeter charges by ~ 16% whilst area increases by 100%. In the previous case when the area quadrupled the perimeter increased three-fold.

Figure A1.7 shows depletion region recombination for all three devices tending to the same limiting value. This result shows that depletion region recombination for these devices is emitter perimeter dependent. The results of Figure A1.6 can be similarly explained by the increase in emitter perimeter combined with the increasing area. Quadrupling length has also increased the perimeter by a similar fraction. The depletion region recombination is taking place in the surface depletion region. Using these results a surface recombination velocity of 2000 $cm.s^{-1}$ has been deduced. Allowing for extra depletion layer widths in lateral pnp transistors and upward operated I^2L gates, this value of surface recombination velocity fits the observed low current behaviour.

PROCESS III DOWNWARD TRANSISTOR

FIGURE A1.8.

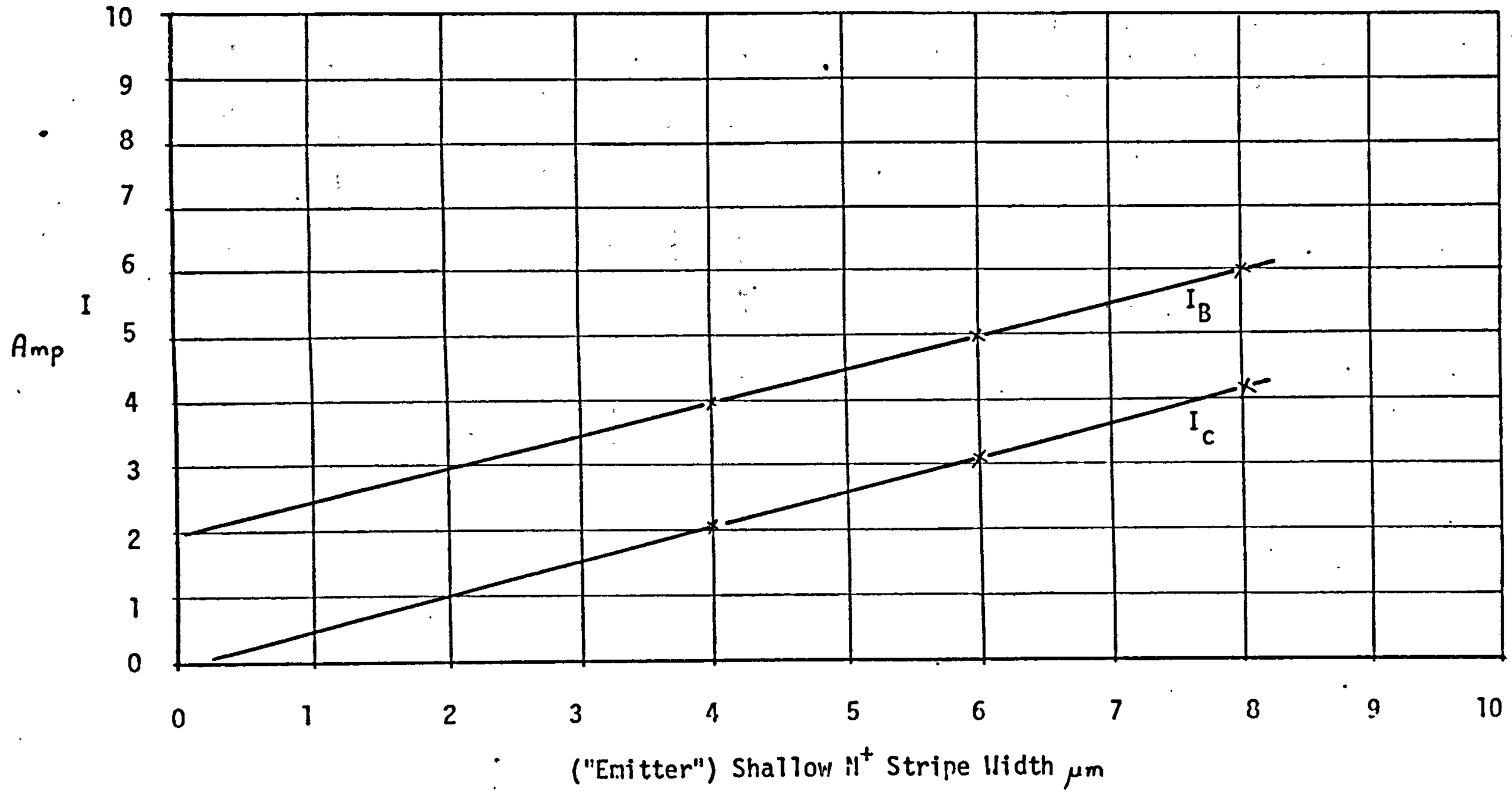
$I_c \times 10^{-5}$

$I_B \times 10^{-7}$

I_c, I_b v Shallow N^+ Width

(V_{be} = 700 mV)

Shallow N^+
20 μm long



Downward transistor gain in medium injection

a) Peripheral Injection

If the characteristics shown in Figure A1.7 are analysed in the medium current range it is found that the collector current at a given V_{be} is directly proportional to shallow N^+ (emitter) stripe width. However, plotting base current against stripe width (Figure A1.8) shows that it is not just proportional to stripe width. At zero stripe width there is a significant base current. This base current is that due to peripheral injection at the shallow N^+ side walls. The data suggests that peripheral injection is 50% of the total base current for a device with a 4 μm wide shallow N^+ stripe. This decreases to 25% for the 12 um wide shallow N^+ device used in I^2L circuits.

b) Gain Variations

Investigating β_d variations of Process III transistors showed at a given temperature and V_{be}, I_B is essentially constant. Figure 6.2. That is, the parameters which control current are nearly independent of gain. The conclusion is that gain variations are due to variations in base transport,

Now

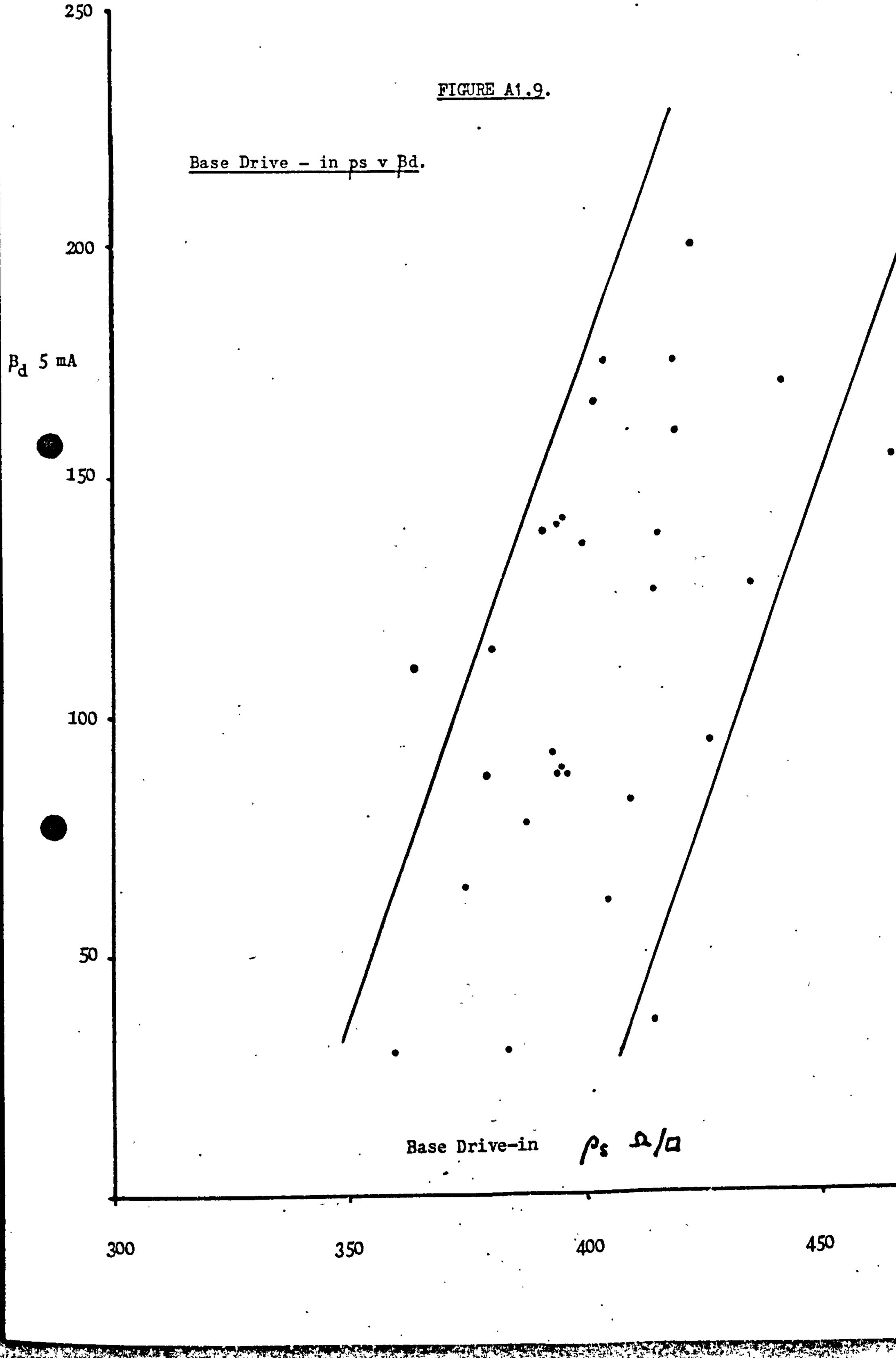
$$\beta_d = \frac{I_C}{I_B}$$

and $$I_B = q \frac{n_i^2 D_n}{\int N_D dx} (\exp (q V/KT)) Ae$$

and $$I_C = q \frac{n_i^2 D_p}{\int N_A dx} (\exp (q V/KT)) Ae$$

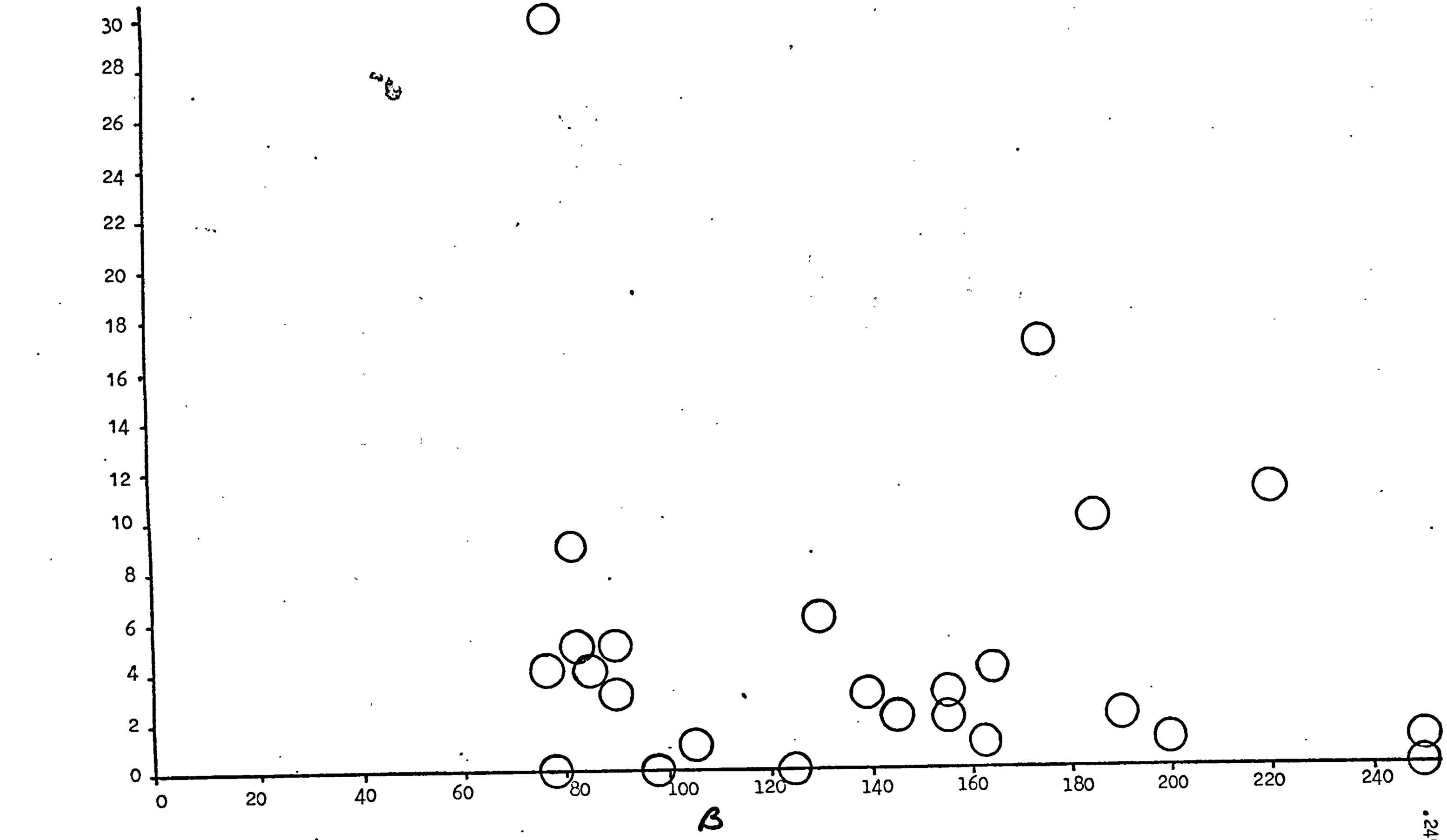
FIGURE A1.9.

Base Drive - in ps v β_d.



% Failure of Test Transistors in Centre slices vs β

FIGURE A1.11



I_B is controlled by the effective integral of the emitter doping $\int N_D\,dx$; this is largely invariant. The integrated base doping $\int N_A dx$ by contrast varies significantly between batches and thus causes gain variants.

In Chapters 3 and 6 it was shown that very precise control of β_d is required in order that I^2L parameters β_u and t_{di} are maintained at optimum values. It has been shown that gain variations are dominated by variations in base transport. Experimental analysis into why base transport is variable showed that the active base doping was very dependent on the sheet resistivity of the base region. Figure A1.9 shows β_d plotted against base diffusion ρ_s. Although there is a pronounced scatter the trend is clear. By comparison the correlation between emitter ρ_s and gain is not clear (Figure A1.10a). As the emitter is a very heavily doped region containing an appreciable fraction of inactive dopant the sheet resistivity (ρ_s) is a poor measure of the total dopant present. To overcome this problem the emitter resistivity test pieces were subjected to an 1100°C activation drive-in. The drive-in ρ_s was then compared with β_d Figure A1.10b. The correlation between β_d and ρ_s is still not evident. Thus it is concluded that base drive-in ρ_s is the major factor controlling gain via its influence on integrated base doping.

Gain and Pipe density

As the formation of a collector emitter pipe is due to

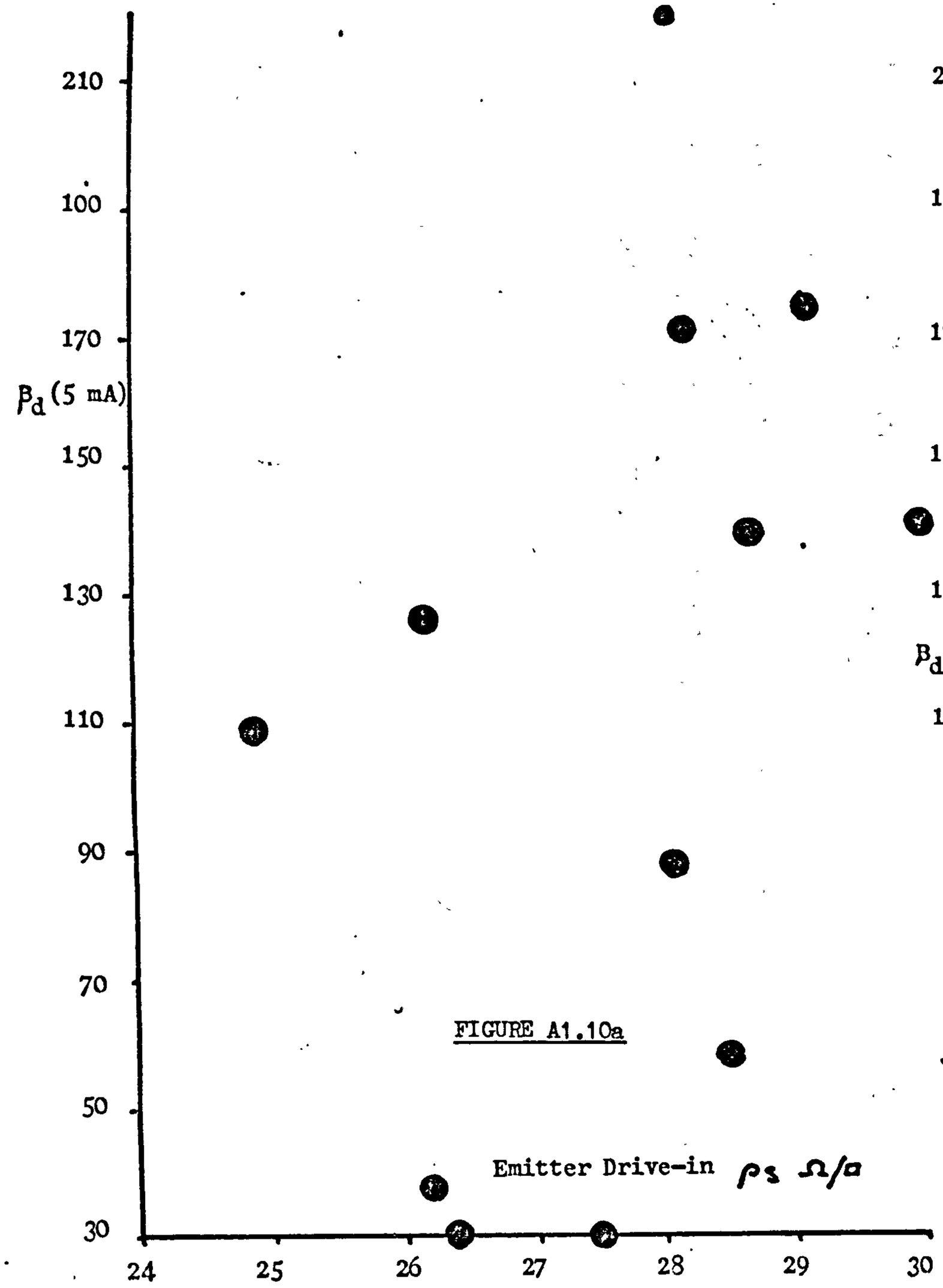


FIGURE A1.10a

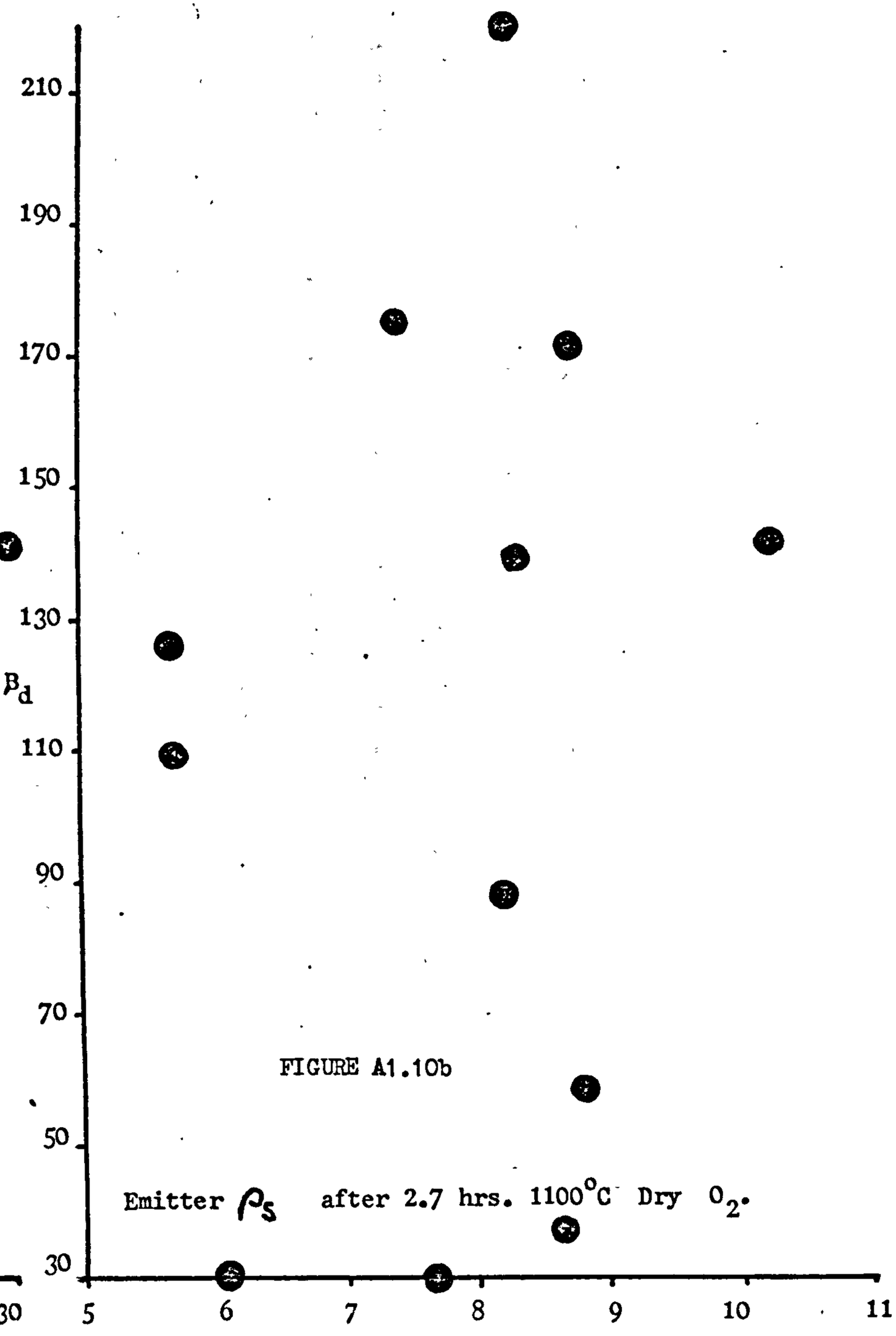


FIGURE A1.10b

the local compensation of base dopant and it has been shown that gain variations are due to variations in integrated base doping, the pipe density as a function of β_d was investigated. Figure A1.11 shows pipe density v β_d. Each data point represents a one hundred device sample from a single wafer. The sample was taken from regions outside slip lobes. The gain is the average for the non-piped transistors in the sample.

The data shows pipe density is independent of gain and hence integrated base doping.

Characterisation data

The remainder of this Appendix details characterisation data for I^2L gates and downward operated devices produced on the I^2L variant of Process III.

PROCESS III I^2L CHARACTERISATION DATA

Percentile Distribution 5mA β d RB20

Percentile Distribution BV_{CEO} RB20 1μA

Percentile Distribution BV_{CBO} RB20 1μA

Percentile Distribution Gate Delay 4-collector gate collector and base contact near injector, injector current 300μA

Percentile Distribution "Emitter base capacitance" 4 collector gate 0v 1MHz.

Percentile Distribution "Collector base capacitance" 12 x 4 μm collector 0v 1MHz

f_T v I_e RB20 V_{cb} = 2V, measurement frequency 200MHz

Probability of yield v β d for pseudo random sequence generator WM7 (see Figure 1.10)

Histogram of maximum frequency WM7 (see Figure 1.10)

V_{ce} v $I_c = I_b$ I^2L output low voltage collector and base near injector 4-collector gate

Gate delay v Gate power temperature as a parameter, single collector gate

V_{ce} sat v temperature $I_b = I_c$ I_b as a parameter

β_u v temperature I_c as a parameter

9 stage single collector ring oscillator; oscillating frequency v temperature, injector current as a parameter

CHART P WELL — Graph Data Ref. 5571 — 80 Equal Divisions x Probability

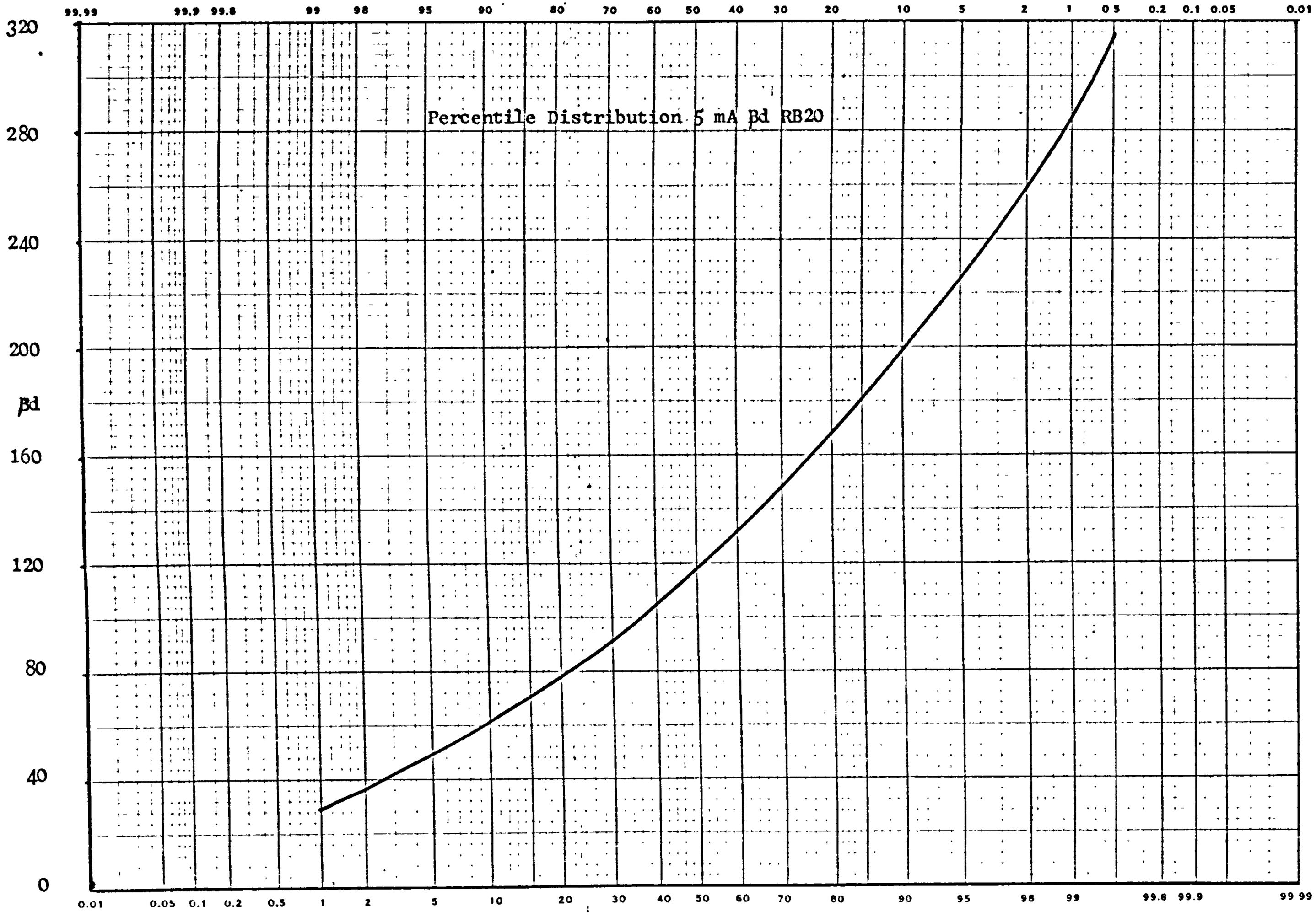
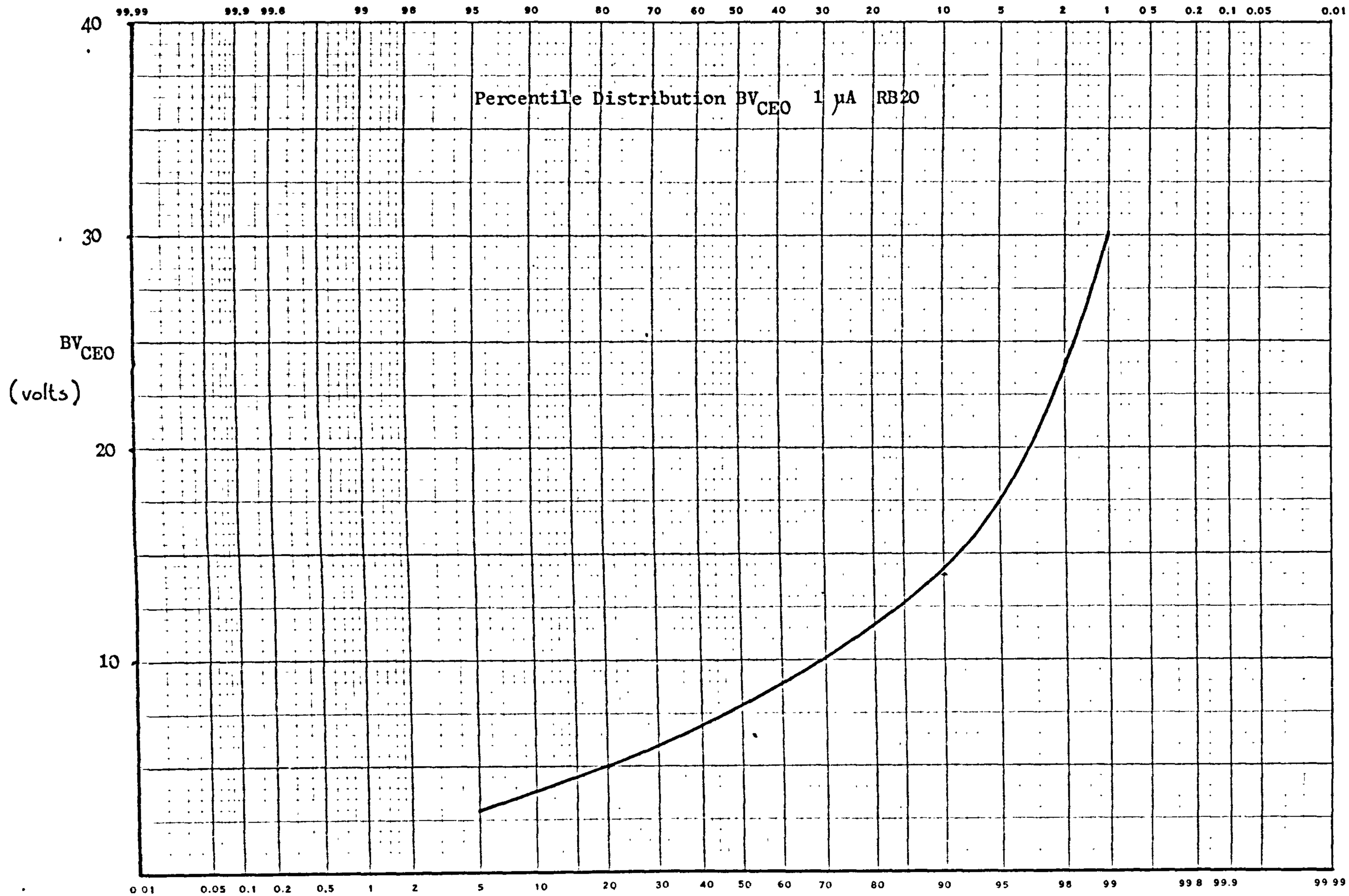


CHART WELL Graph Data Ref. 5571

80 Equal Divisions x Probability



PERCENTILE DISTRIBUTION BV_{CBO} 1 μA

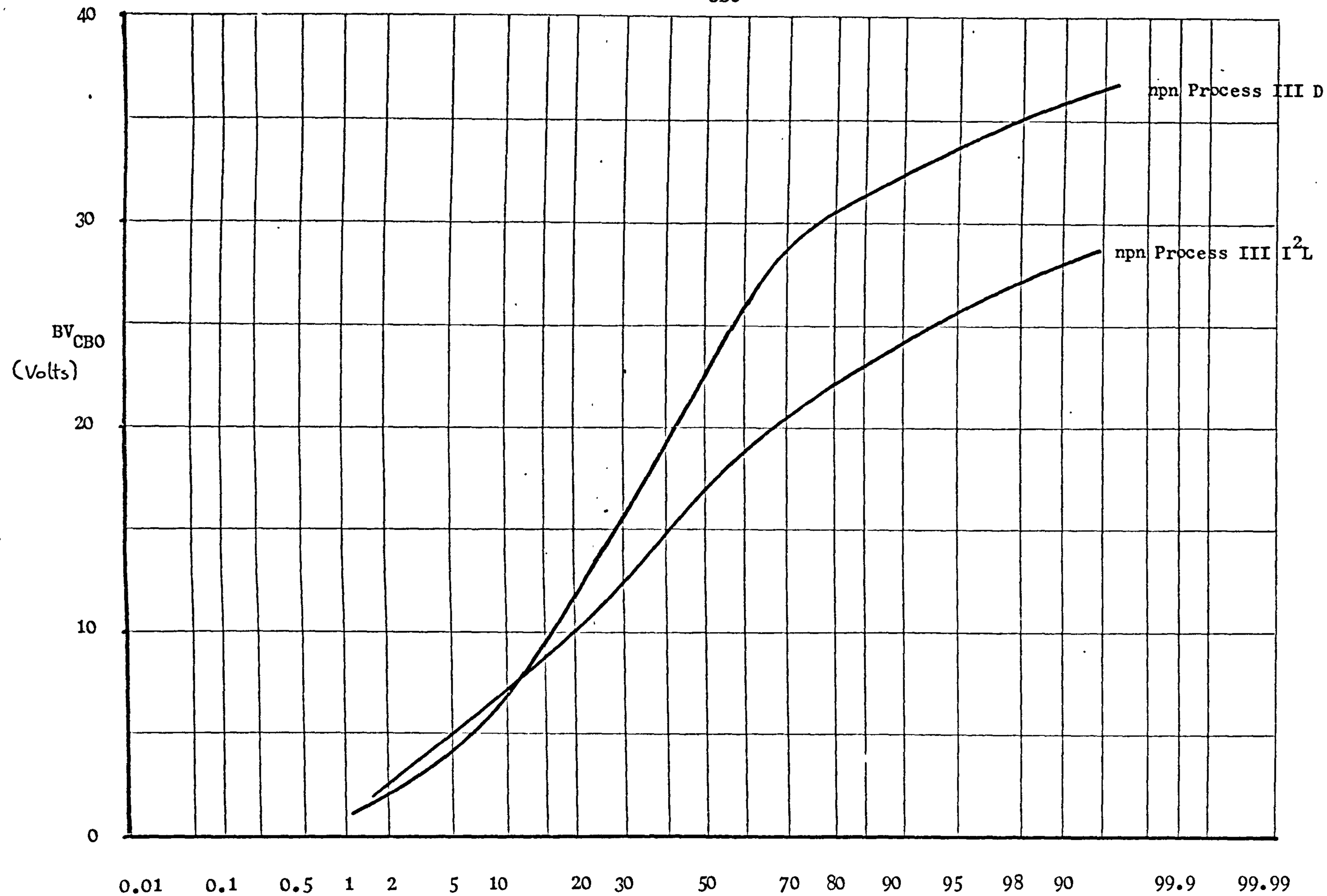
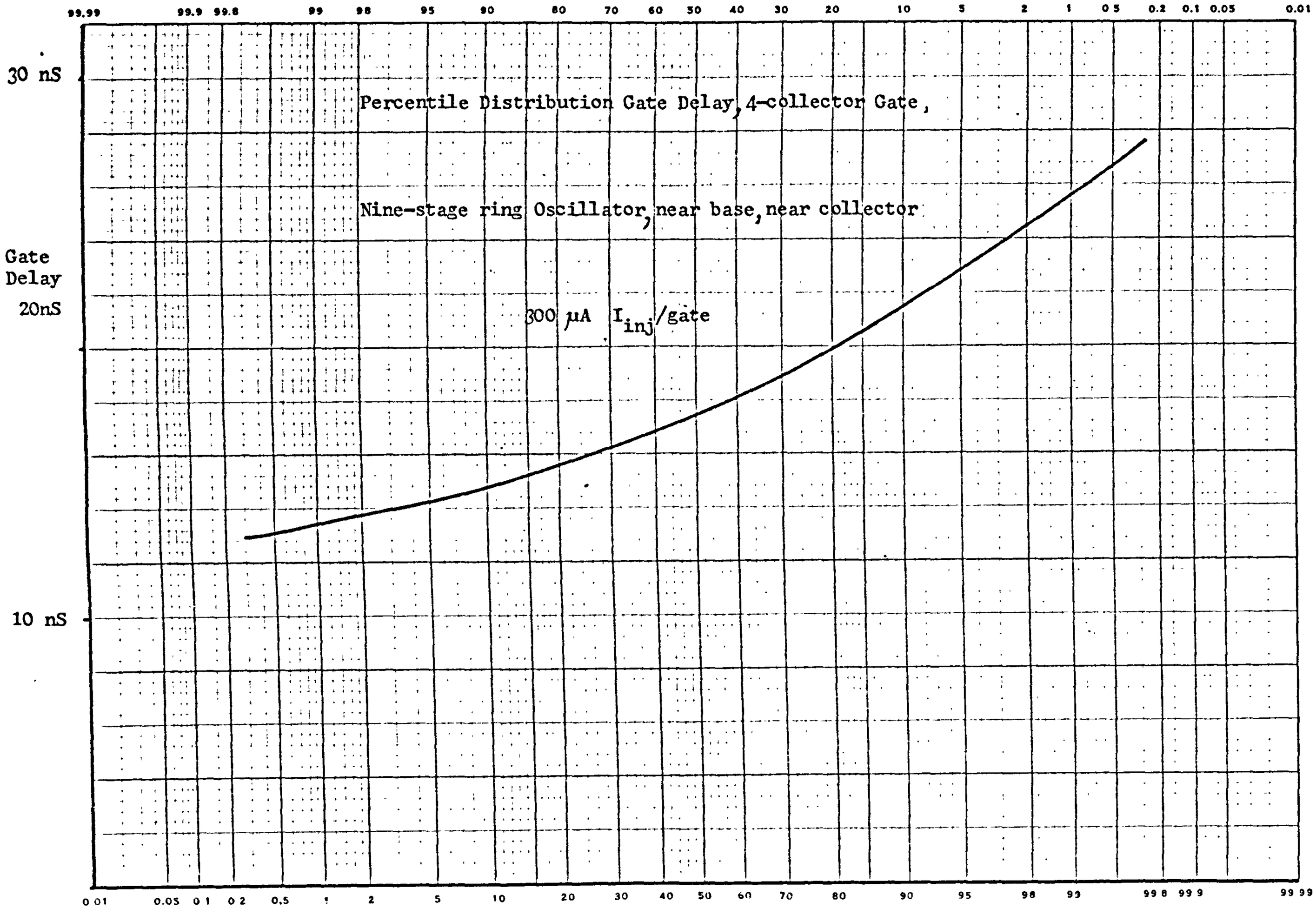


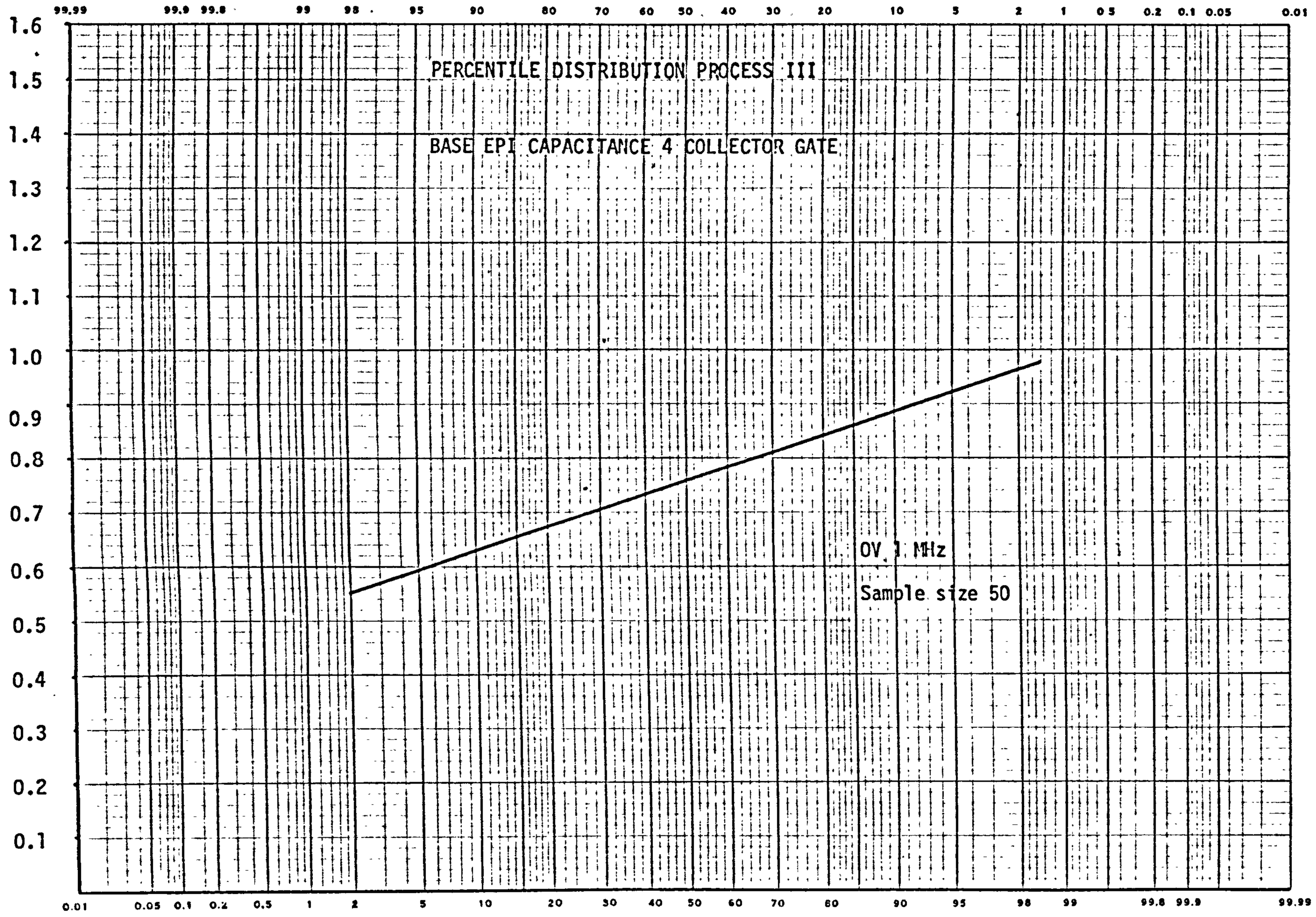
CHART WELL Graph Data Ref. 5571 80 Equal Divisions x Probability



WELL

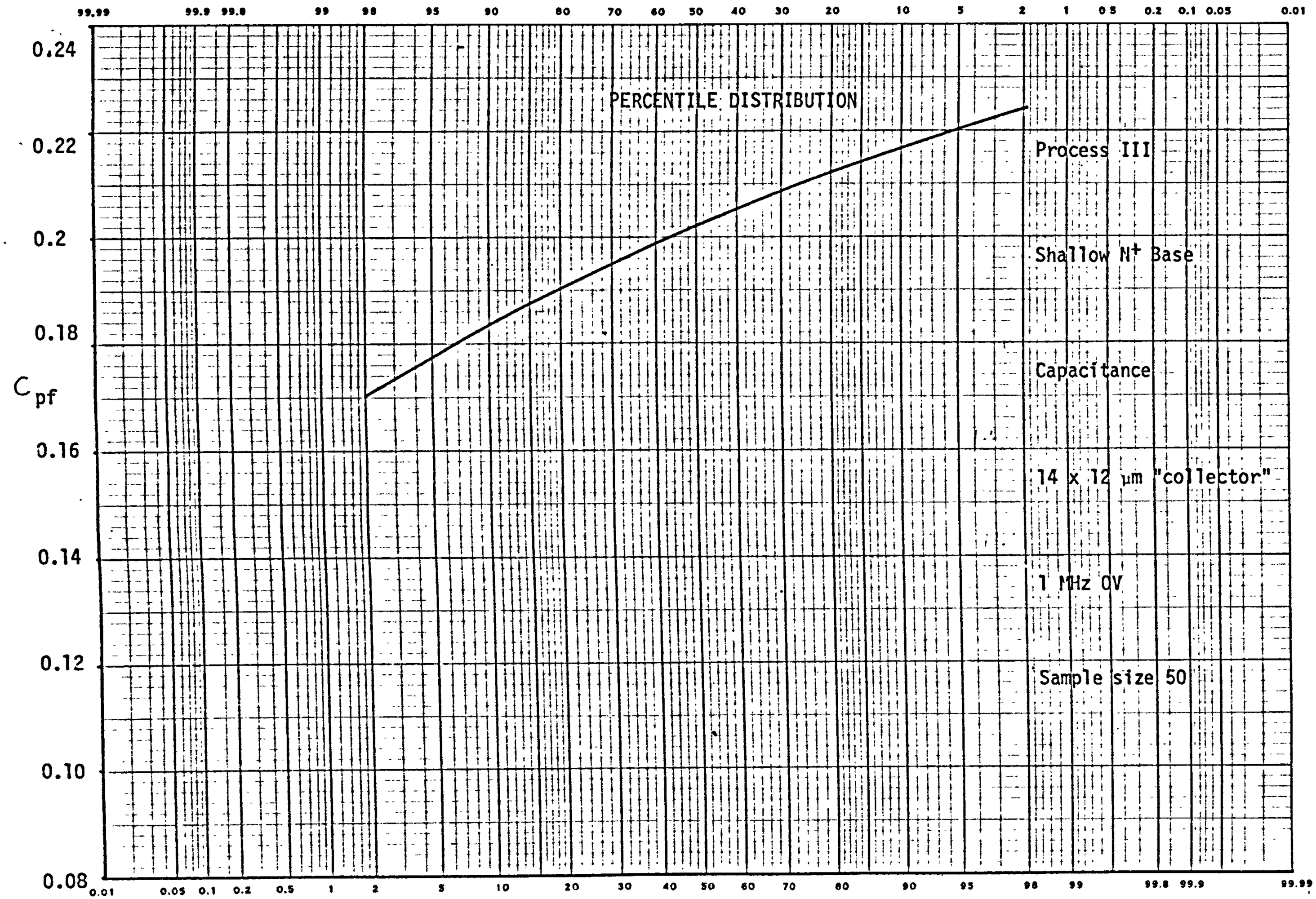
Graph Data Ref. 5571

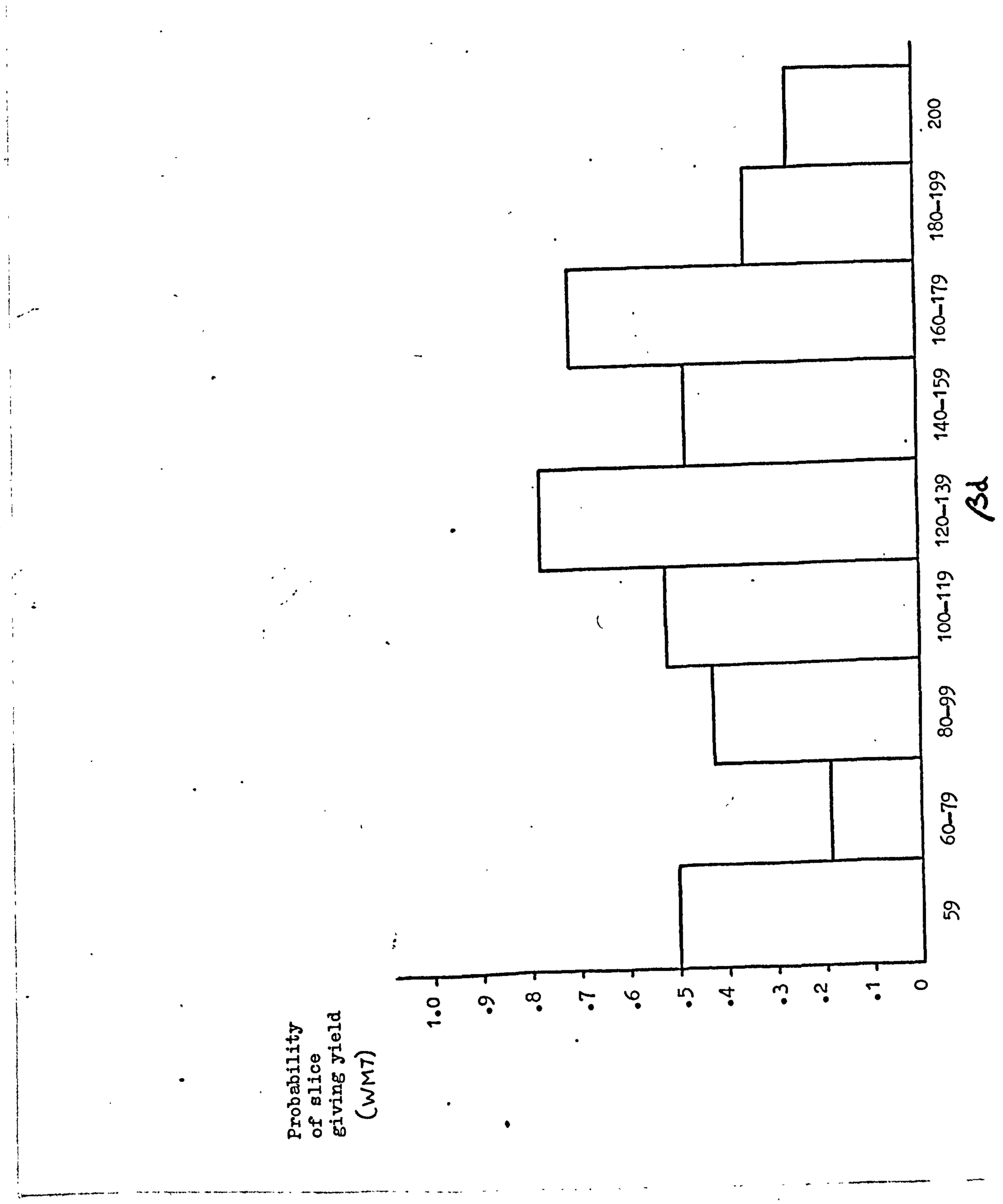
80 Equal Divisions x Probability



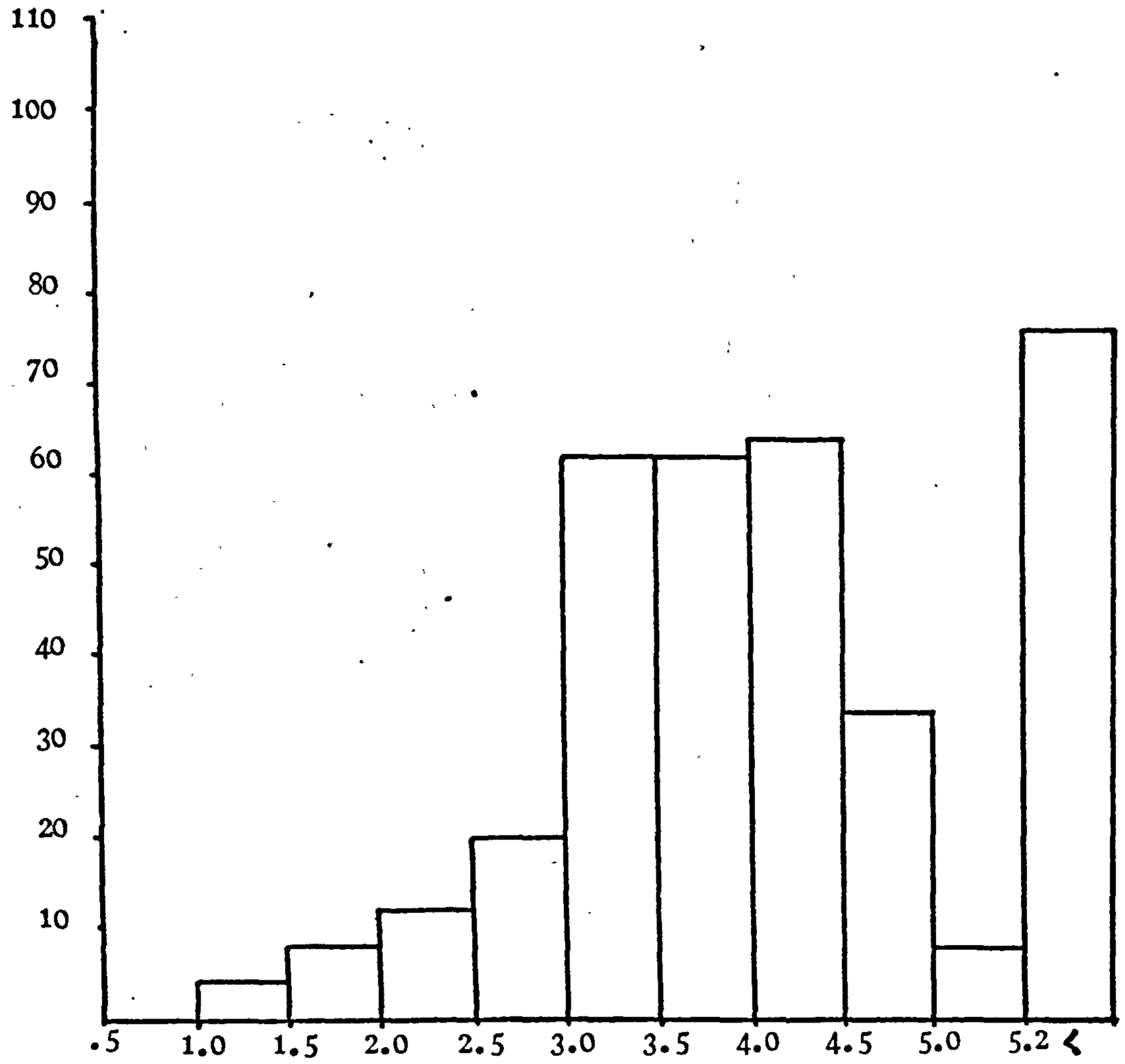
Graph Data Ref. 5571

80 Equal Divisions x Probability




Probability of slice giving yield (WM7)
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
59
60–79
80–99
100–119
120–139
140–159
160–179
180–199
200
Bd

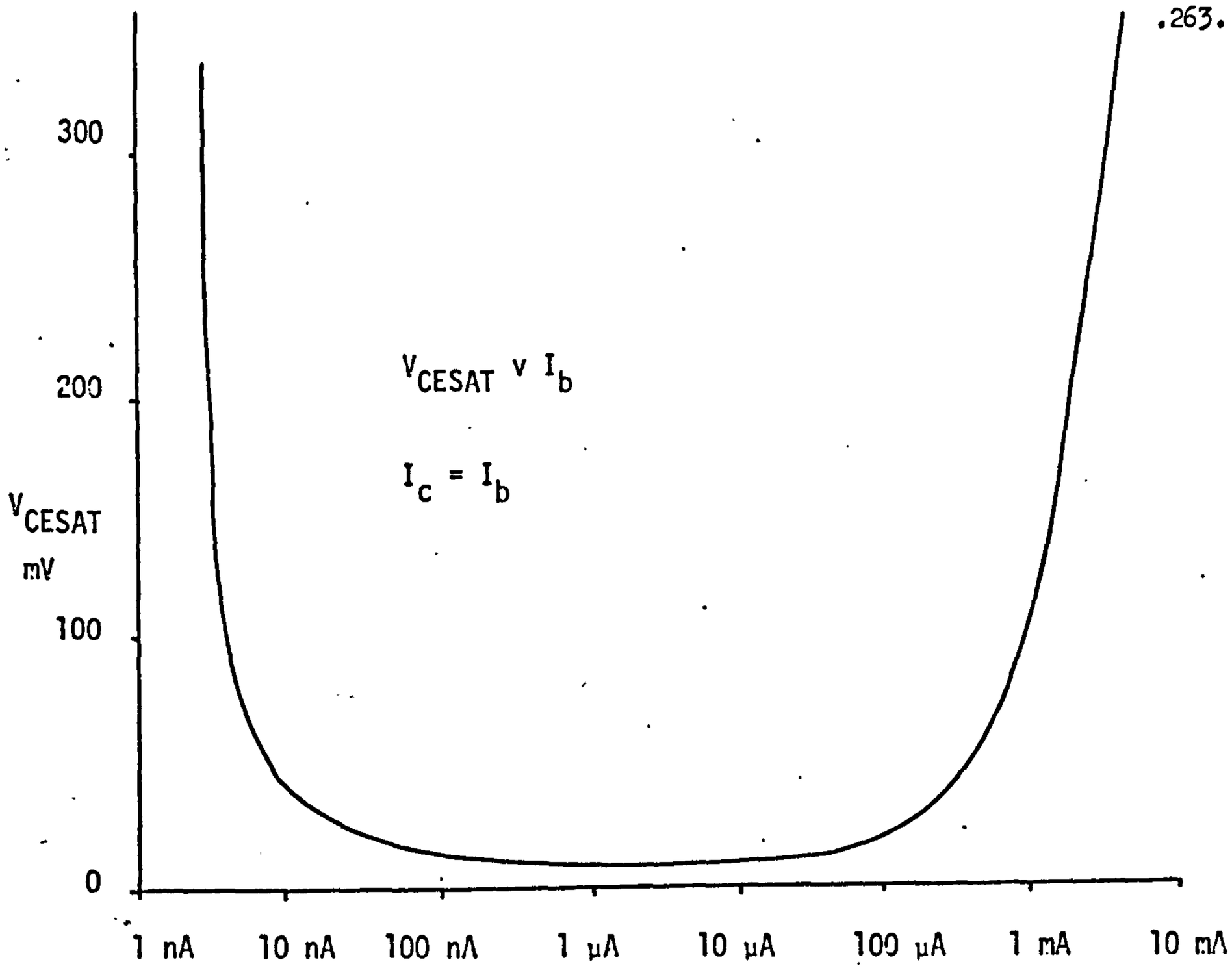
HISTOGRAM WM7 MAXIMUM OPERATING FREQUENCY
(Sample 355 Devices)



FREQUENCY MHz

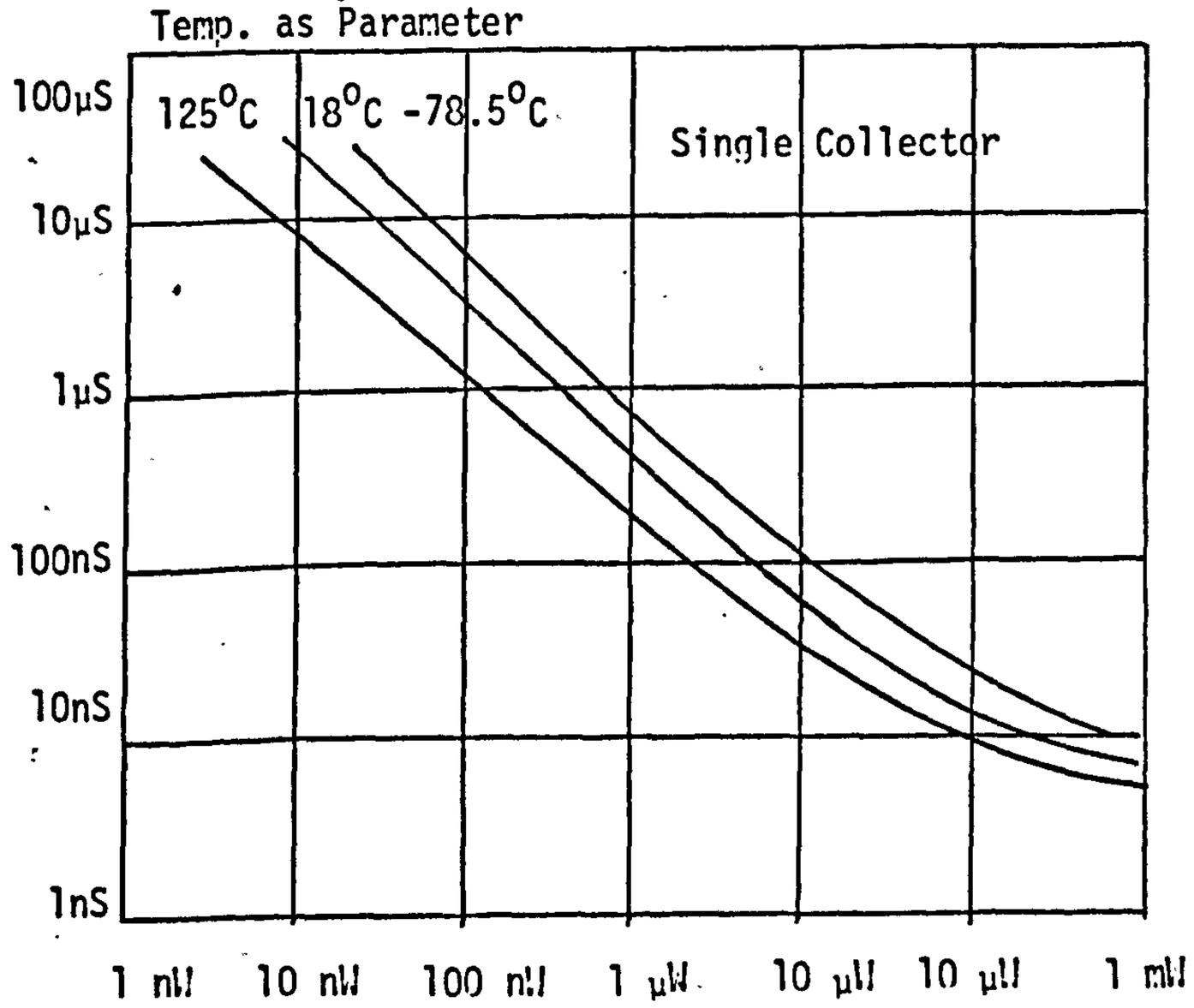
V_{CESAT} v I_b

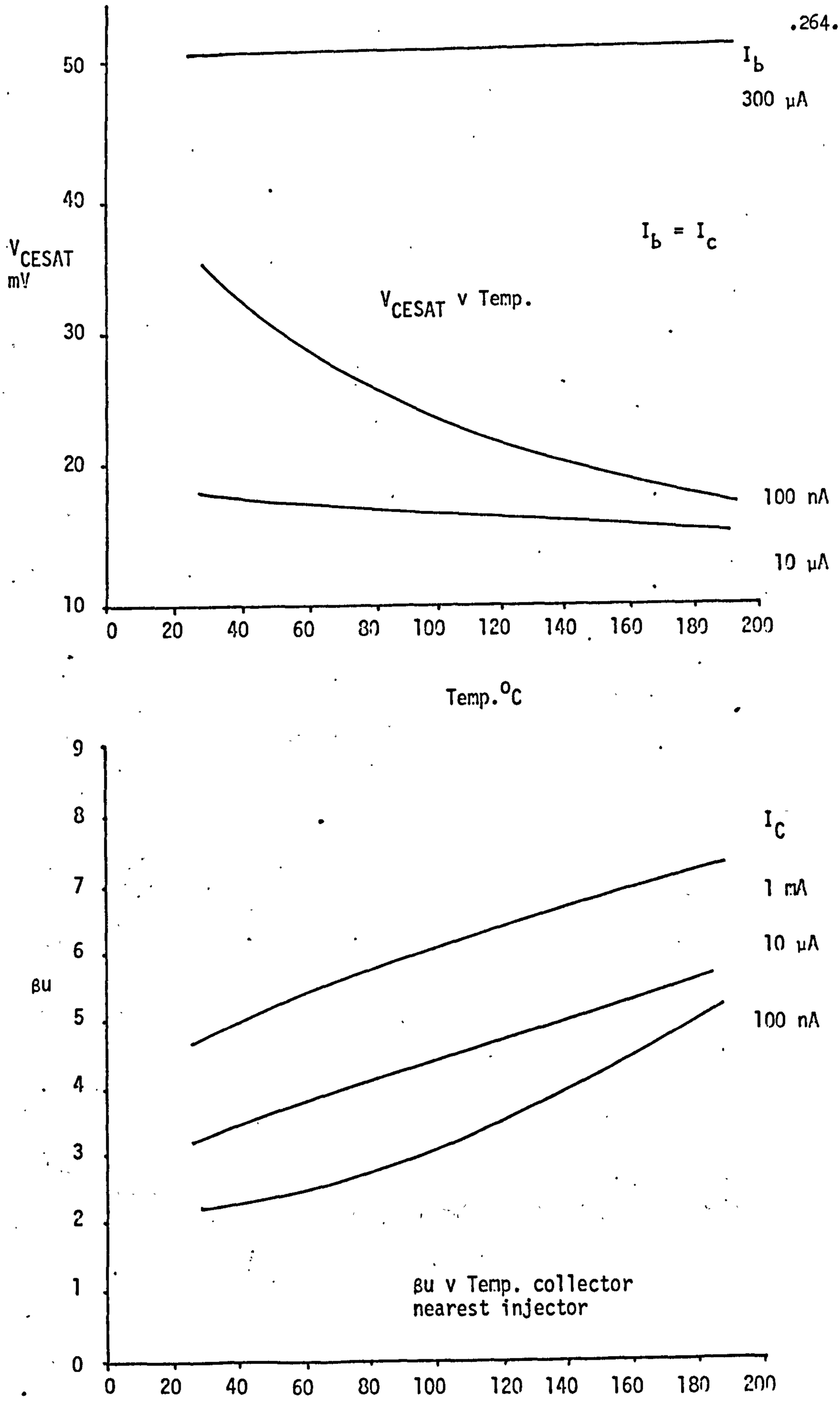
$I_c = I_b$



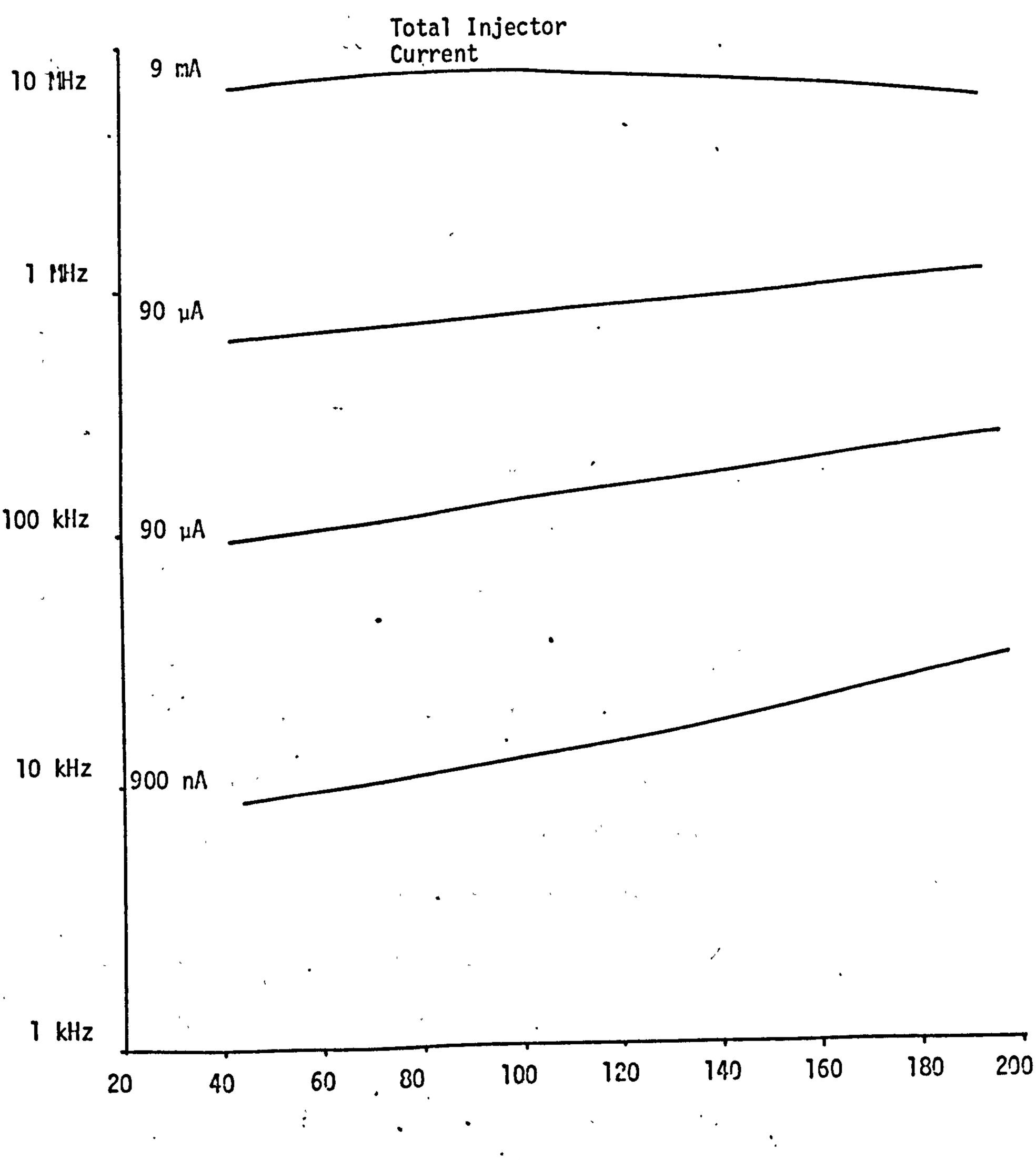
I_b

Gate Delay v Gate Power
Temp. as Parameter




50
40
30
20
10
V_{CESAT} mV
I_b
300 µA
$I_b = I_c$
V_{CESAT} v Temp.
100 nA
10 µA
0 20 40 60 80 100 120 140 160 180 200
Temp. °C
9
8
7
6
5
4
3
2
1
0
βu
I_C
1 mA
10 µA
100 nA
βu v Temp. collector
nearest injector
0 20 40 60 80 100 120 140 160 180 200
Temp. °C

9-STAGE SINGLE COLLECTOR RING OSCILLATOR
OSCILLATING FREQUENCY V TEMP.



APPENDIX 2

PROCESS D AND H

Processes D and H, although they are distinctly different processes, are of similar construction. Process D is optimized for production engineering and the manufacture of bipolar integrated circuits for the consumer market. Process H is optimized for manufacturing circuits required to operate in hostile high voltage environments. This includes control functions for electrical machinery. The process is only required to fulfil low speed applications.

The layout of the Process D I^2L gate is shown in Figure A2.1; collectors 16 x 18 μm, lateral pnp base width is 12 μm drawn.

The proposed layout of the Process H I^2L gate is shown in Figure A2.2. This is similar to the Process D gate except a shallow N^+ region is placed across the surface of the lateral pnp injector transistor. The shallow N^+ region eliminates minority carrier injection in the surface region of the injector transistor. The device now functions only on the transport between the buried N^+ and shallow N^+. The transport in this region is large due to the thick epitaxy on Process H. In order for I^2L to operate the efficiency of the pnp must be reduced. This is to eliminate the re-injection component of the npn base current.

The salient characteristics of Process D and Process H are listed in Table A2.1.

TABLE A2.1

	PROCESS D	PROCESS H
Substrate	1 Ω cm P (111)	2.5 Ω cm P (111)
Buried	10 Ω/sq. Arsenic	10 Ω/sq. Arsenic
Epitax	1 Ω cm 10.5 μm	4 Ω cm 17 μm
Isolation	30 Ω/sq. 14 μm xj	30 Ω/sq. 22 μm xj
Collector	3 Ω/sq. 7 μm xj	3 Ω/sq. 10 μm xj
Base	200 Ω/sq. 2.5 μm xj	220 Ω/sq. 3 μm xj
Emitter	4.5 Ω/sq. 2.2 μm xj	4.5 Ω/sq. 2.5 μm xj

FIGURE A2.1.

CONSUMER PROCESS I^2L GATE

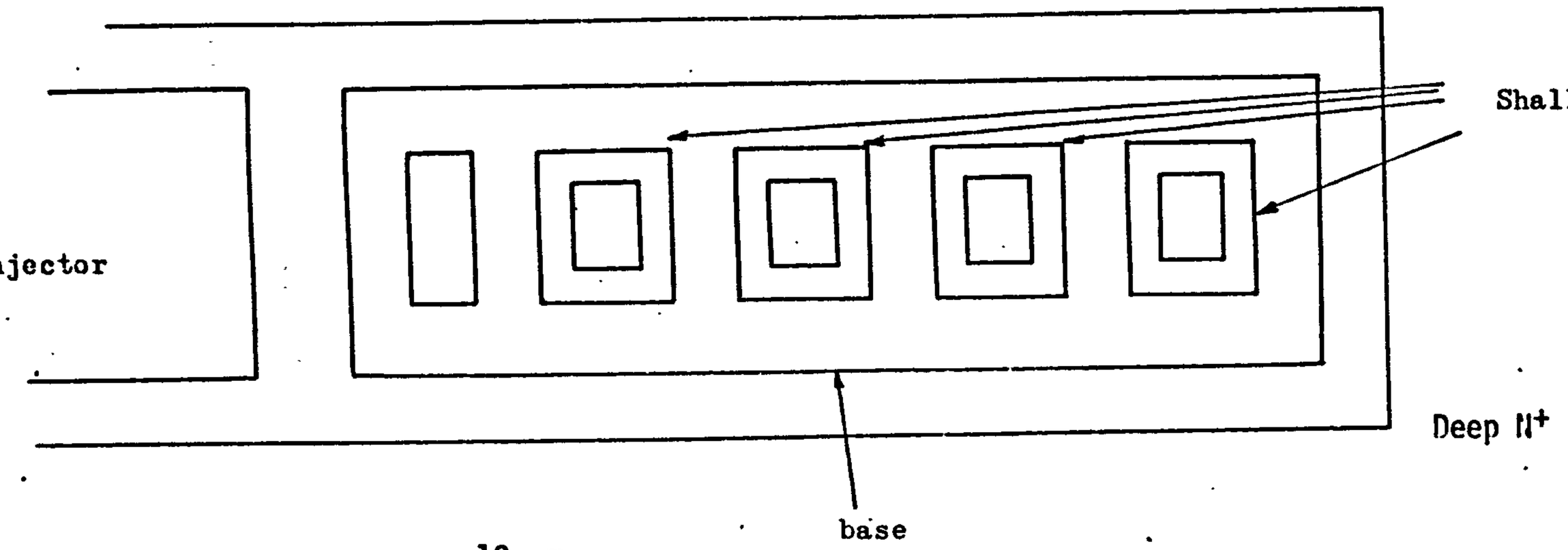
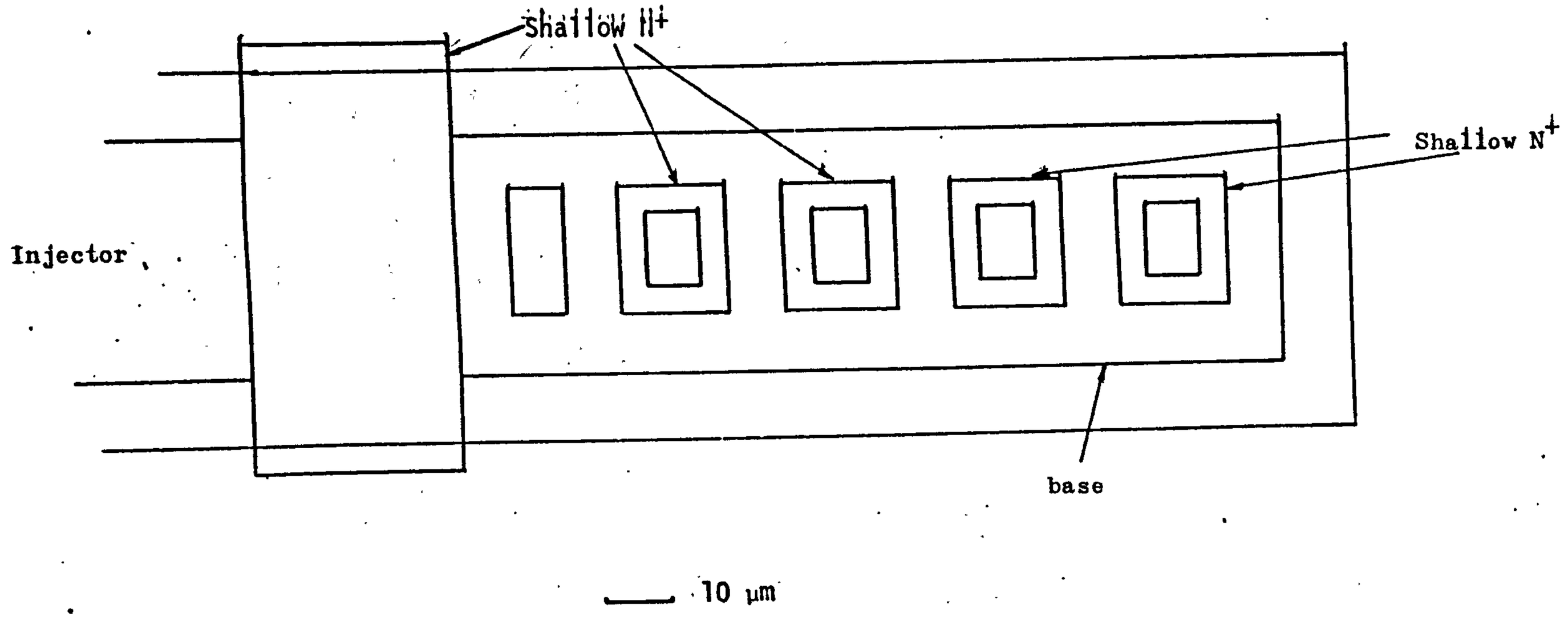


FIGURE A2:2

HIGH VOLTAGE PROCESS PROPOSED GATE STRUCTURE



APPENDIX 3

PROCESS III I^2L TEST MASK WT45.

1. SB 410
2. RB 20
3. Ring Oscillator using 'bare collectors' and all-over base.
4. Ring Oscillator using 'Re-cut collectors' and all-over base.
5. Ring Oscillator using 'Re-cut collectors' standard base.
6. Ring Oscillator using 'bare collectors' standard base.
7. Gate structure for investigating nature of $Si-SiO_2$ interface and effect on base currents.
8. D-type as divide by 2 'bare collector' P.E. defined base.
9. D-type as divide by 2 'Re-cut collectors' P.E. defined base.
10. D-type as divide by 2 'Re-cut collectors' P.E. defined base.
11. D-type as divide by 2 'bare collectors' all-over base.
12. IBM-type 4-bit memory cells.
13. Four-collector gate ring oscillator 'Re-cut collector' P.E. defined base.
14. Four-collector gate ring oscillator 'bare collectors' P.E. defined base.
15. Dual 'bare collector' gates, four collectors per gate, all-over base.
16. Dual 'Re-cut collectors' gates, four collectors per gate, all-over base.
17. 'Bare collector' four-collector gates with separate injectors, one with staggered land. P.E. defined base.
18. 'Re-cut collector' four-collector gates with separate injectors, one gate with staggered land P.E. defined base.
19. Four-bit memory cell using 'bare collectors' and all-over base.
20. Dual four-collector gate 'Re-cut collector' P.E. defined base.
21. Dual four-collector gate 'bare collector' P.E. defined base.
22. Dual four-collector gate 'Re-cut collector' P.E. defined base, Interdigital Injector.
23. Dual four-collector gate 'bare collector' P.E. defined base Interdigital Injector.

(P.E. abbreviation Photo-engraving)

FIG A3.1

PHOTO - MICROGRAPH WT 45 A

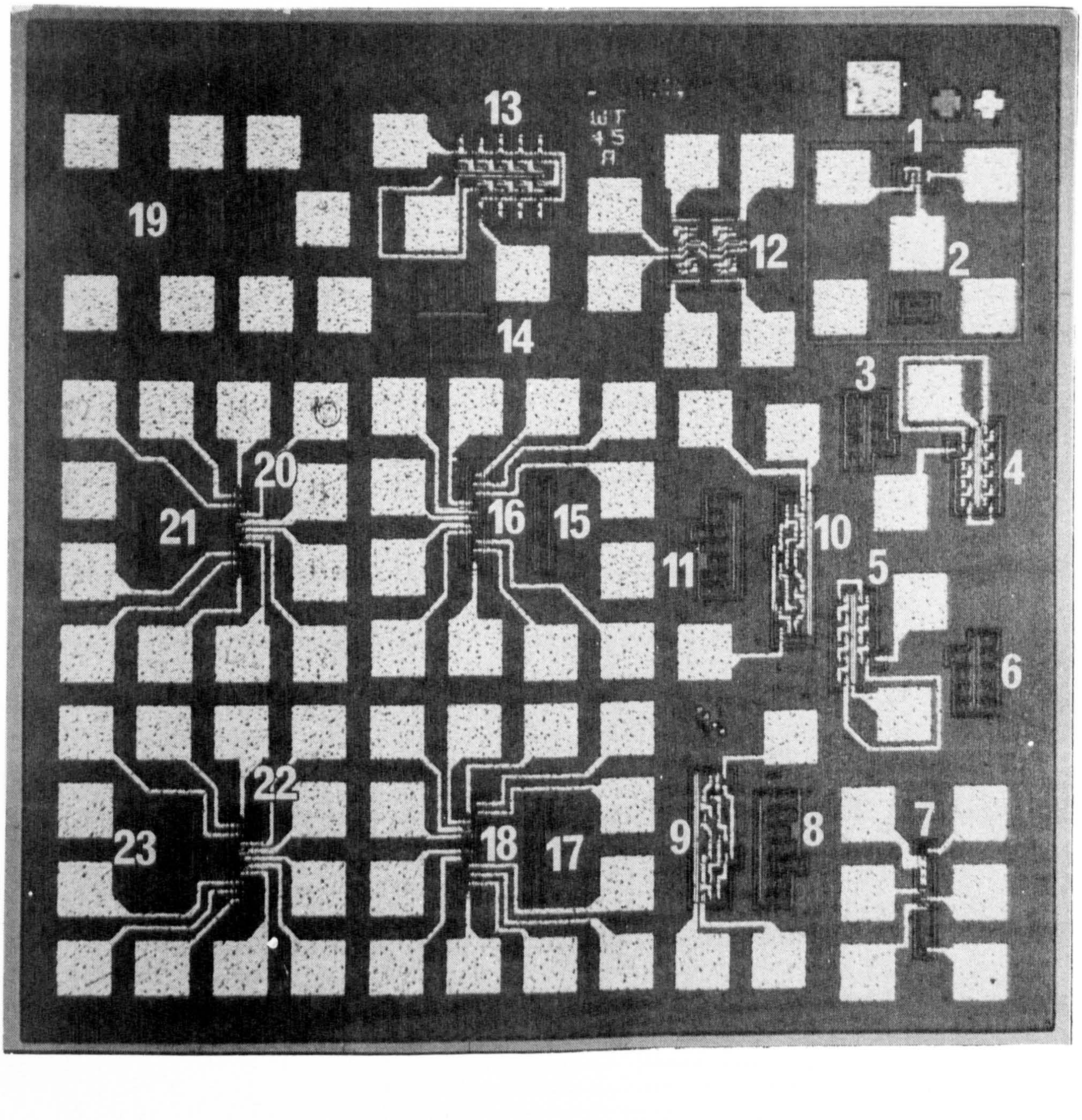


FIG. A3.2(a)

COMPARISON OF STANDARD

AND INTERDIGITATED I^2L GATES ON PROCESS III

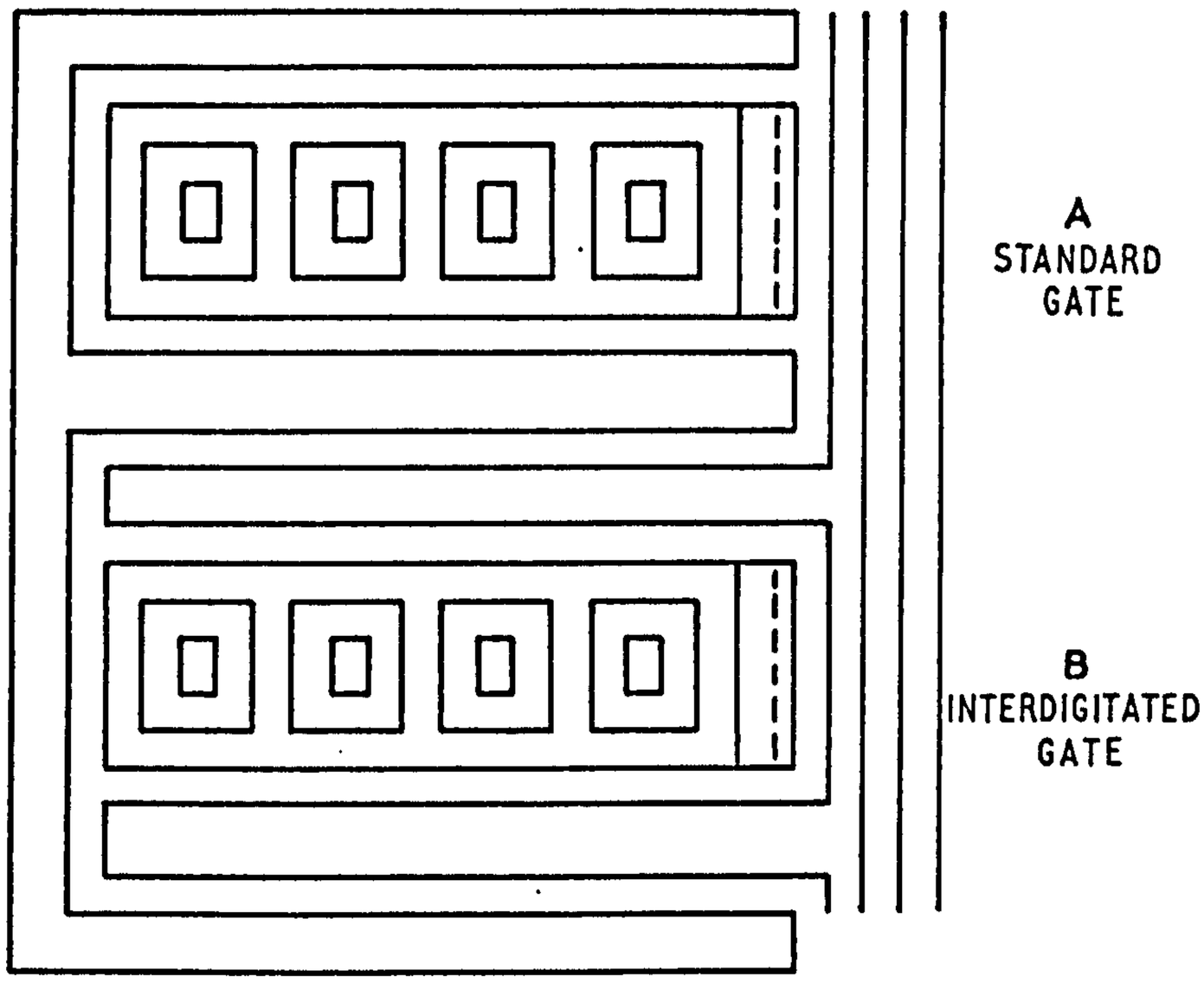
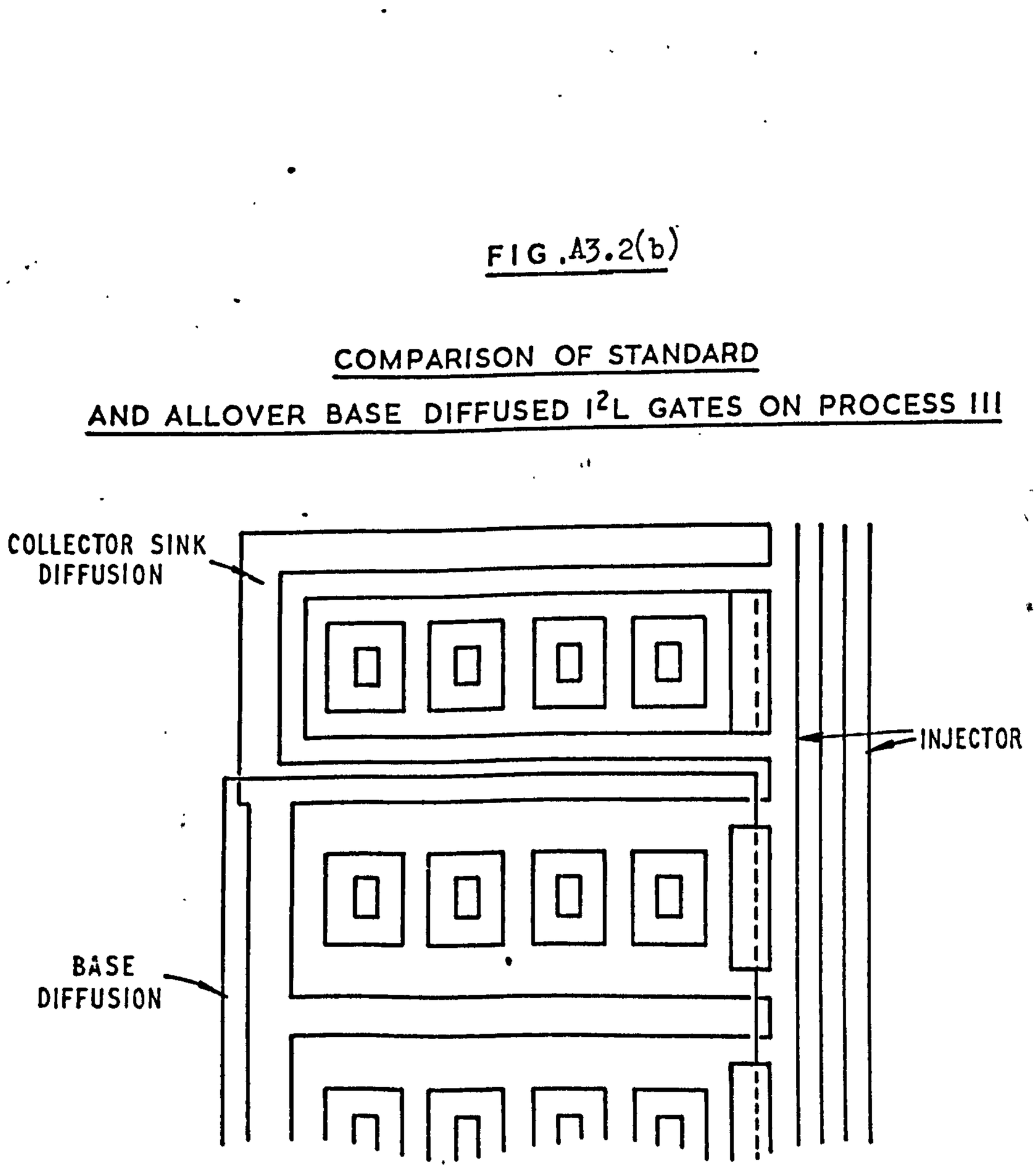


FIG. A3.2(b)

COMPARISON OF STANDARD

AND ALLOVER BASE DIFFUSED I^2L GATES ON PROCESS III



APPENDIX 4

WM4 CONTENTS

1) Weidmann Berger diagnostic structures

2) 5, seven gate single collector ring oscillators

3) 4, seven gate 4 collector ring oscillators

4) 223 gate 4 collector ring oscillator

5) 99 gate 4 collector ring oscillator

6) 16 bit D-element shift register

7) R, 2R resistor ladder network for D to A conversion

8) 4, npn transistor with experimental anti-saturation clamps

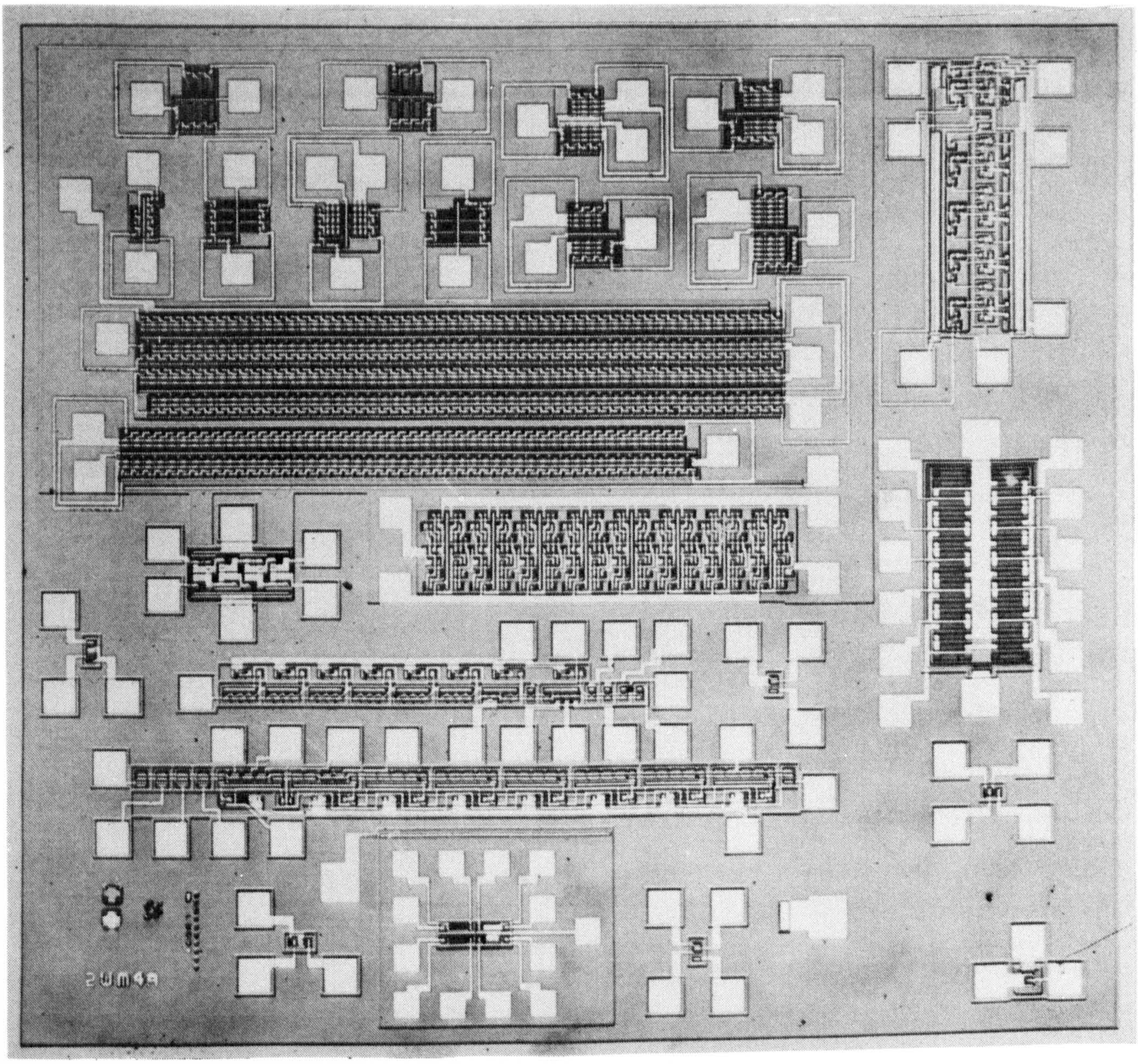
9) standard lateral pnp and planar npn transistors

10) 2 conventional transistor test circuits

11) Experimental shift register using clocked injectors

12) I^2L test structure using stacking. One I^2L level on top of another. Injector current of the bottom level being fed from the N^+ land of the top land. Both levels isolated.

Mask Designers - L.W.Kennedy and G.W.Sumerling.



APPENDIX 4 PROCESS III I^2L TEST MASK WM4

FIGURE A4.1

APPENDIX 5

M693 CONTENTS

Four collector Test gates.

1) 16 x 16μm collectors

   16μm base width injector

   12μm base width injector

   10μm base width injector

2) 20 x 26μm collector

   12μm base width injector

3) Weidmann Berger diagnostic structures

4) 16 x 16μm collector gate with shallow N^+ replacing deep N^+

5) D- element shift register

   8 bits 16 x 16μm collectors

   8 bits 16 x 20μm collectors

6) 12 seven gate 4 collector ring oscillators to evaluate power delay product and minimum gate delay

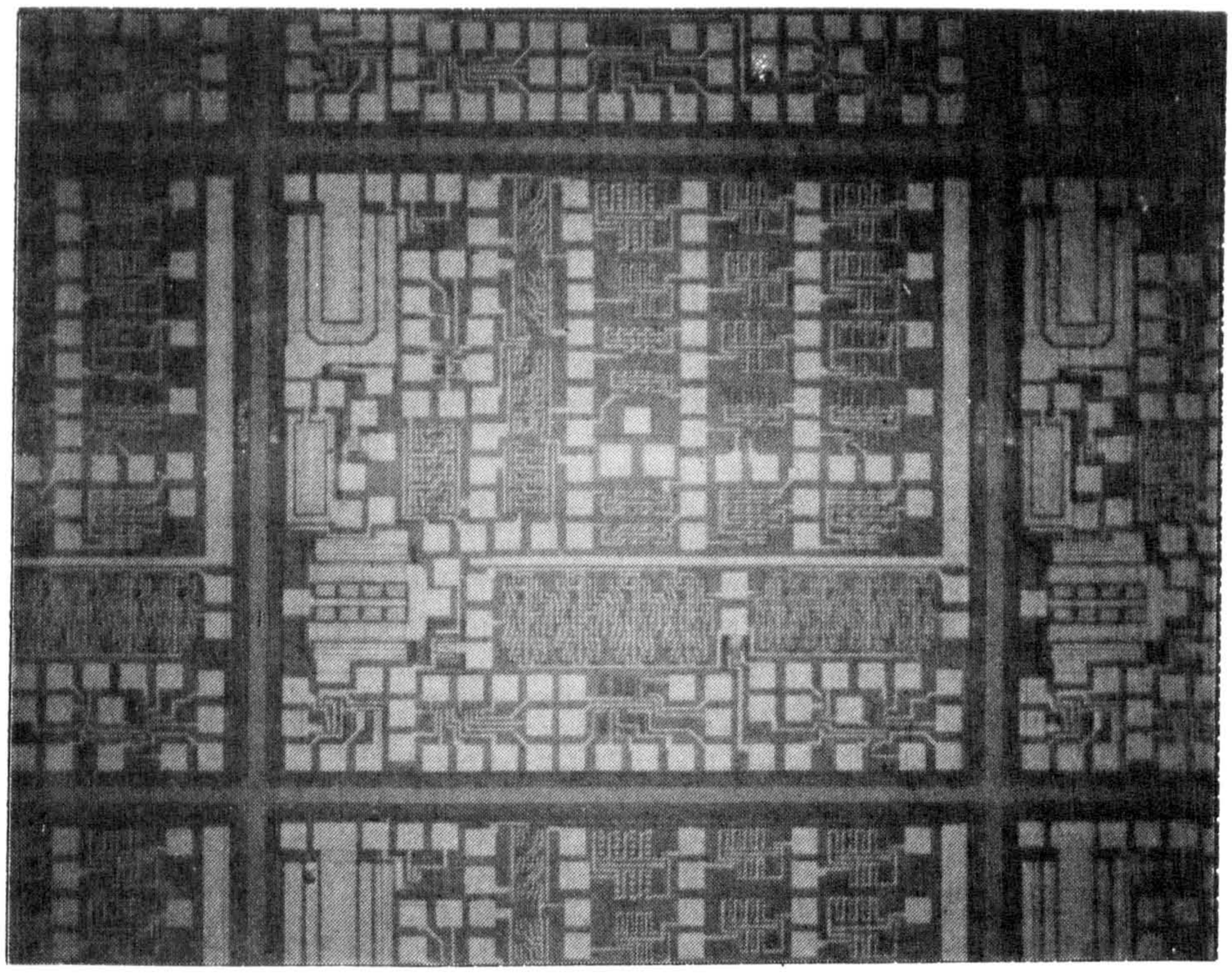
7) 4 seven gate single collector ring oscillators to evaluate power delay product and minimum gate delay.

8) Shift register structures after Lagerberg (IEE First European Solid State Circuits Conference 2-5 Sept.1975)

9) Standard lateral pnp and planar npn transistors

10) Power pnp and power npn transistors

Mask Designers L.W.Kennedy and A. Brittain.



APPENDIX 5 PROCESS D AND H I^2L TEST
MASK M689

FIGURE A5.1

APPENDIX 6

Relevant publications by the Author

European Solid State Device Research Conference
University of Sussex 12-15 September 1977.
Paper B1.6"Piece-wise Injection model of the

I^2L gate"

L.W.Kennedy

Proceedings of IEEE Vol.65 No.2, February 1977, page 272
"B.J.T. Field Factor Measurement and the Ebers Moll Reciprocity Condition"

B.L.Hart
R.W.J. Barker
L.W.Kennedy

151st Meeting Electrochemical Society
Philadelphia, Pennsylvania, May 8-13 1977
Recent News Papers Electronics Division.
"Defects and Pipes in Shallow Diffused Bipolar Transistors"
Paper 453 RNP

L.W.Kennedy
K.D.Perkins

I^2L Colloquim organised by IERE and IOP London
London 1st 1976. Royal Institution, Albemarle St. London

L.W.Kennedy "I^2L Engineering"

IEEE Journal of Solid State Circuits, 1975, Vol.SC-10 No.5 pp.336
"Substrate Fed Logic"

V.Blatt
P.Walsh
L.W.Kennedy

University of Leuven, Belgium.
Semiconductor Device Course June 1st-4th, 1976
"I^2L on a Shallow Diffused Bipolar Process"

L.W.Kennedy

APPENDIX 7

HEAVY DOPING

7.1. ENERGY GAP NARROWING

A heavily doped semiconductor is one in which the assumption of discrete impurity levels associated with doping is no longer valid. This is because the impurity states have broadened into impurity bands. The effect of the impurity band is to modify the distribution of states in the conduction band in an n-type semiconductor. (Valence band in a p-type semiconductor). This is because the impurity band overlaps the main band.

The basic assumption in the theoretical treatment of heavily doped semiconductors is that the total number of states in the main band is unaltered as a result of the impurity band. The major modification to the material is a reduction in the width of the energy gap. As the reduction in the energy gap is doping dependent it varies throughout the structure of real bipolar devices. Thus the energy gap in the emitter may be significantly different from that in the intrinsic and extrinsic base regions. This energy gap difference is possibly responsible for many of the temperature characteristics of silicon bipolar devices. The effective hole electron product n_{ie}^2 now becomes

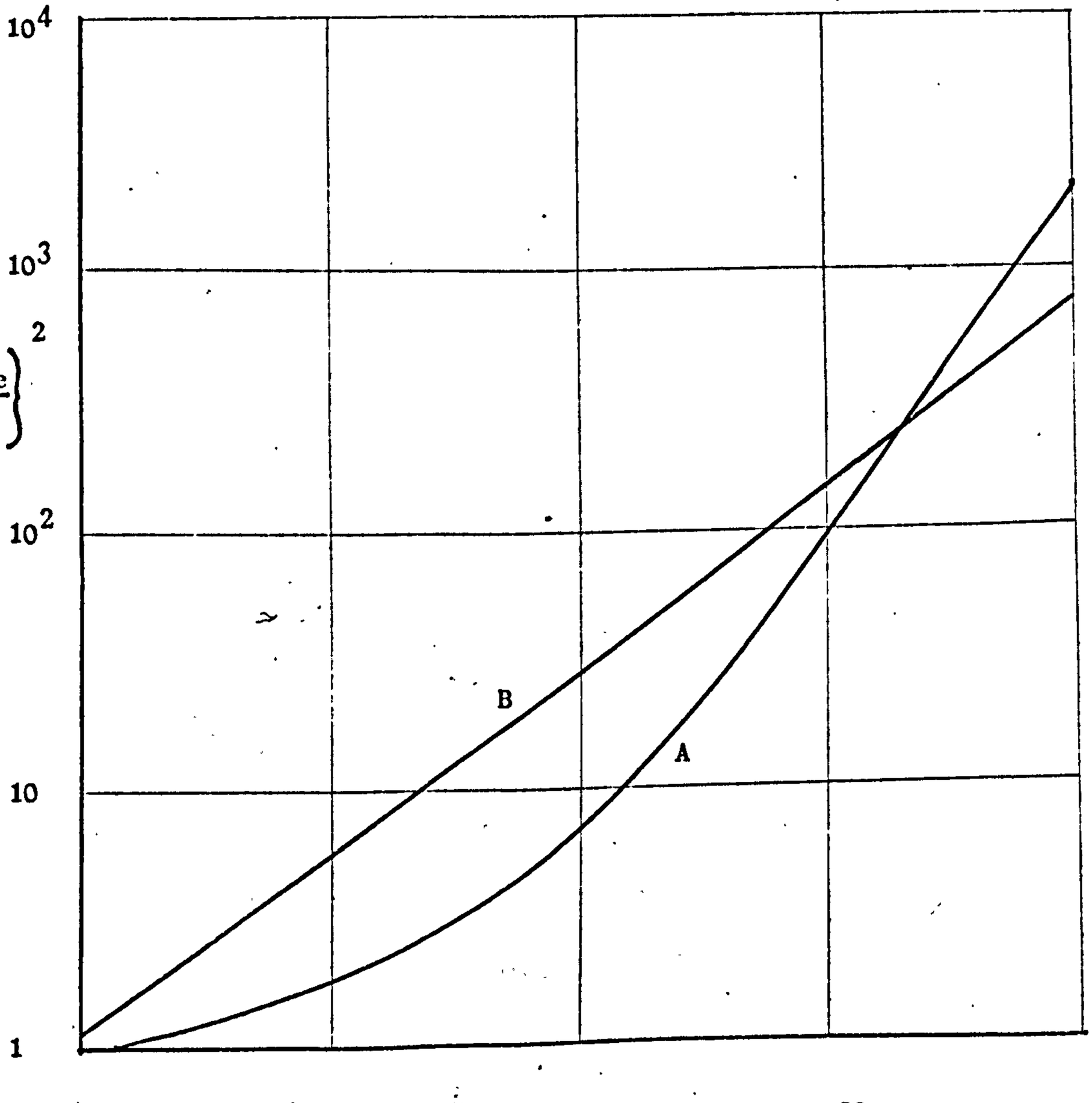
$$n_{ie}^2 = np = 1.5 \times 10^{33} T^3 \exp - (E_g - \Delta E_g)/KT$$

Where ΔE_g is the energy gap shrinkage.

The hole electron product n_i^2 in silicon without energy gap narrowing is: $n_i^2 = 1.5 \times 10^{33} T^3 \exp - (E_g/KT)$ (ref 39 page 51)

FIGURE 7.11

Effective Intrinsic Carrier Concentration as a Function of Doping



A after Mock (32)

B after Slotboom and de Graaf

Slotboom and de Graaf (33) have made extensive experimental investigations of the temperature behaviour of the base of silicon bipolar transistors. The devices used had base doping in the range $4 \times 10^{15} - 2.5 \times 10^{19} cm^{-3}$(Boron). The result of the investigations was an expression for the energy gap narrowing due to high boron concentrations

$$\Delta E_g = 9 \times 10^{-3}(\ln (N/10^{17}) + (\ln^2(N/10^{17}) + 0.5)^{1/2}) \text{ eV}$$

The ratio of the effective hole electron product in a heavily doped material to the lightly doped case is then:-

$$\left(\frac{n_{ie}}{n_i}\right)^2 = \exp \left(\Delta E_g/KT \right)$$

For the sake of simplicity it can be considered that the doping in heavily doped regions is reduced by this factor.

Now

$$n = \frac{n_i^2}{N_A} \exp (qV/KT), \text{lightly doped case}$$

therefore

$$n = \left(\frac{n_{ie}}{n_i}\right)^2 \cdot \frac{n_i^2}{N_A} \exp (qV/KT), \text{heavily doped case}$$

We can define therefore an effective doping

$$N_{A\ \text{effective}} = N_A \cdot \left(\frac{n_i}{n_{ie}}\right)^2$$

In the calculation of minority carrier levels in all heavily doped regions of the I^2L gate, viz. extrinsic base, and buried N^+, the treatment of Slotboom and de Graaf has been used. The observed experimental behaviour of the gate is predicted closely by using this treatment, although the buried N^+ is arsenic, not boron doped. (Figure A7.1).

7.2. MINORITY CARRIER LIFETIME

In order to predict the injected currents into heavily doped semiconductors, accurate information regarding minority carrier lifetime is essential. The I^2L gate structure does allow some measurement of the diffusion length in the buried N^+, and as the mobility data available is reasonably accurate, minority carrier lifetimes can be calculated.

The Weidmann Berger gate structure allows for the measurement of hole injection into the epitaxial layer of the I^2L gate. If the recombination in the epitaxial layer is small, this hole current is that incident at the buried N^+ - epitaxial interface. If the I^2L gate is fabricated on a p-type substrate the hole current transported across the buried N^+ can be measured as collected current at the buried N^+ substrate junction. Approximating the buried N^+ as a uniform doped region, and then using long base diode theory, we obtain:-

$$J_{p1} = qD_p \frac{n_{ie}^2}{N_D} \exp(qV/KT) \cdot \frac{\coth}{L_p}(W/L_p)$$

where J_{p_1} is the injected current density incident on the buried N^+

N_D buried N^+ doping

W buried N^+ width

L_p diffusion length in buried N^+

D_p diffusion coefficient in the buried N^+

(see ref 39 page 106)

and

$$J_{p_2} = q\, D_p\, \frac{n_{ie}^2}{N_D}\, \exp(qV/KT).\ \frac{1}{L_p \sinh(W/L_p)}$$

J_{p_2} is the hole current density collected at the buried N^+ substrate junction.

$$\frac{J_{p1}}{J_{p2}} = \cosh(W/L_p)$$

J_{p_1}, J_{p_2}, and W are easily measurable.

Now $$\tau_{\text{Buried } N^+} = \frac{1}{D_p} \left\{ \frac{W}{\text{arc cosh} \left(\frac{J_{p1}}{J_{p2}} \right)} \right\}^2$$

Using this method, buried N^+ lifetimes of 20nS have been observed on Process III. (N_D average $4 \times 10^{18} cm^{-3}$).

Beck and Conradt (4 4) have measured the Auger recombination coefficients in n and p-type heavily doped material. The value of minority carrier lifetime observed in Process III buried N^+ is consistent with their data. As the observed buried N^+ lifetimes agree with that of Beck and Conradt, their data was used to calculate minority carrier lifetime in all heavily doped regions.

$$\tau_n = \frac{1}{1.7 \times 10^{-31} \times N_D^2} \qquad \text{n-type}$$

$$\tau_p = \frac{1}{1.2 \times 10^{-31} \times N_A^2} \qquad \text{p-type}$$

Lifetimes of ~ 40 us were observed in the lightly doped samples measured.

The measurements of Beck and Conradt were performed on

bulk samples. A real transistor will contain diffused or ion implanted regions containing measurable amounts of crystal damage. Lifetimes are likely therefore to be less than those predicted, especially for regions of very heavy doping.

REFERENCES TO CHAPTERS 1 to 6 AND APPENDICES

1) P.W.Cook, D.L. Critchlow and L.M. Terman, Comparison of MOSFET Logic Circuits, IEEE Journal of Solid State Circuits p.348-355, Vol. SC8 October 1975.

2) F.F. Fang and H.S. Rupprecht, High Performance MOS Integrated Circuit using the Ion Implantation Technique. IEEE Journal of Solid State Circuits, p.205-211, Vol. SC.10, August 1975.

3) MOSFET IN CIRCUIT DESIGN, R.H.Crawford. Texas Instruments Electronic Series - McGraw-Hill 1967

4) J.L. Buie and D.R. Breuer, A Large-Scale Integrated Correlator, IEEE Journal of Solid State Circuits, p.357-363, Vol. SC.7 October 1972.

5) G.W. McIver, R.W. Miller, T.G. O'Shaughnessy, A Monolithic 16 x 16 Multiplier. Solid State Circuits Conference, Philadelphia, February 1974.

6) Integrated Circuits Design Principles and Fabrication. Editors R.M. Warner Jr., J.N. Fordemwalt, McGraw-Hill Motorola Series in Solid State Electronics, p.138.

7) B.T. Murphy, V.J. Glinski, P.A. Gary and R.A. Pedersen, Collector Diffusion Isolated Integrated Circuits, Proceedings of the IEEE Vol.57, No.9, September 1969.

8) V.A. Dhaka, J.E. Muschinske and W.K. Owens, Subnanosecond emitter-coupled logic gate circuit using Isoplanar II, IEEE Journal of Solid State Circuits, Vol.SC.8, October 1973.

9) H.H. Berger and S.K. Wiedmann. Merged-Transistor Logic (MTL) IEEE Journal of Solid State Circuits, Vol.SC.7, October 1972 p.340-346.

10) K. Hart and A. Slob, Integrated Injection Logic, IEE Journal of Solid State Circuits, Vol.SC.7, October 1972, p.346-351.

11) R.E. Grippen, D.O'Brien, K. Rallapalli and P.W.J.Verhofstadt. High Performance Integrated Injection Logic, A Microprocessor Sequencer Built with I^3L, IEEE Journal of Solid State Circuits p.662-668, Vol. SC.11, October 1976.

12) H.H. Berger and S.K. Wiedmann. Terminal Orientated Model for Merged Transistor Logic (MTL). IEEE Journal of Solid State Circuits p. 211-217, Vol. SC.9, October 1974

13) S.K. Wiedmann. Injection-Coupled Memory. A High-Density Static Bipolar Memory. IEEE Journal of Solid State Circuits Vol. SC.8, October 1973

14) H.H. Berger. The Injection Model A Structure-Orientated Model for Merged Transistor Logic MTL. IEEE Journal of Solid State Circuits, p.218-227, Vol. SC.9, October 1974.

15) F.M. Klaasen, Device Physics of Integrated Injector Logic, IEEE Transactions on Electron Devices, P.145-152, Vol. ED.22, March 1975.

16) H.E.J. Walms. Base Current of I^2L Transistors, IEEE Journal of Solid State Circuits, p.143-150, Vol. SC.12, April 1977.

17) S.C. Choo, Theory of a Forward-Biased Diffused-Junction P-L-N Rectifier Part I Exact Numerical Solutions. IEEE Transactions on Electron Devices, p.954-966, Vol. ED.19 August 1972.

18) N.H. Fletcher. The High Current Limit for Semiconductor Junction Devices, Proc. I.R.E. p.862-872, June 1957.

19) J.B. Gunn. On carrier accummulation and the properties of certain semiconductors junction. J. Electronic Control p.17, Vol.4, 1958.

20) R.W. Dutton and R.J. Whittier, Forward Current-Voltage and Switching Characteristics of P^+NN^+ (Epitaxial) Diodes, IEEE Transactions on Electron Devices, p.458-467, Vol. ED.16, May 1969.

21) A.B. Phillips, Transistor Engineering, Mc Graw-Hill Series on Solid State Engineering, 1962.

22) C.T. Sah, R.N. Noyce, W. Shockley. Carrier Generation and Recombination in P-N Junctions and P-N Junction Characteristics. Proc. I.R.E. p.1228-1243, Sept. 1957.

23) D.E. Fulkerson, Solid State Electronics, p.821-826, Vol.11, 1968.

24) S. Chou, Solid State Electronics, p.811-826, Vol.14, 1971.

25) A. Hertlett, The Forward Characteristic of Silicon power rectifiers at High current densities. Solid State Electronics, p.717-742, Vol.11, 1968.

26) W.H. Matthews, University of Leuven, Belgium. Private communication July 1976.

27) G.W. Ludwig and R.L. Watters. Drift and Conductivity Mobility in Silicon Physics Review, p.1699-1701, Vol.101 March 1956.

28) E.M. Conwell and V.F. Weisskopf, Physics Review, p.388, Vol. 77, 1950.

29) H. Brooks. Electrical Properties of Germanium and Silicon in "Advances in Electronics and Electron Physics". Vol. V11 p. 156-160, Academic Press Inc. New York, 1955.

30) D.C. Scharfetter and H.K. Gummel, Large-signal analysis of a silicon Read diode oscillator, IEEE Transactions on Electron Devices, p.64-77, Vol. ED.16, January 1969.

31) R.J. Van Overstraeten, H.J. Demann and R.P. Mertens, Transport Equations in Heavy Doped Silicon. IEEE Transactions on Electron Devices, p.290-298, Vol. ED.20, March 1973.

32) M.S. Mock, Transport Equations in Heavily doped Silicon and the current Gain of Bipolar Transistors. Solid State Electronics, p.1251-1259, Vol.16, 1973.

33) J.W. Slotboom and H.C. De Graaf, Measurements of Bandgap narrowing in Silicon Bipolar Transistors. Solid State Electronics, p.857-862, Vol.19, 1976.

34) B. Lewis, Arsenic Auto doping of silicon epitaxial layers. Plessey Technical Report, 1975.

35) A.S. Grove, O. Leistiko and C.T. Sah, Redistribution of Acceptor and Donor Impurities During Thermal Oxidation of Silicon. Journal of Applied Physics, 35 2695 (1964).

36) J.C. Irvin , Resistivity of Bulk Silicon and of Diffused Layers in Silicon, p.387-410, Vol. XL1, March 1962. The Bell System Technical Journal.

37) J.L. Moll and I.M. Ross. The Dependence of Transistor Parameters on the Distribution of Base Layer Impurities. Proc. I.R.E. 44 72.

38) A.S. Grove. Physics and Technology of Semiconductor Devices, Wiley Interscience, 1967.

39) A.B. Phillips. Transistor Engineering, McGraw-Hill Series in Solid State Engineering, 1962.

40) S.S. Shinozaki, T. Iizuka, F. Masuoka, K. Shinada, J. Miyamoto. Role of the External Base Region of the n-p-n Transistor on the Switching Speed of Integrated Injection Logic (I^2L). IEEE Journal of Solid State Circuits, p.185-191, Vol. SC.12 April 1977.

41) N.C. de Troye. Integrated Injection Logic Present and Future. IEEE Journal of Solid State Circuits, p.206-211, Vol. SC.9, October 1974.

42) S.M. Sze, Physics of Semiconductor Devices, Wiley Interscience, 1969.

43) H.K. Gummel. Measurement of the number of Impurities in the Base Layer of a Transistor. Proc. I.R.E. 49 834, 1961.

44) J.D. Beck and R. Conradt. Auger recombination in Silicon, Solid State Communications, Vol.13, p.93-95, 1973.

REFERENCES TO CHAPTER 7.

1) Integrated Circuits Design Principles and Fabrication. Editors R.M. Warner Jr. and J.N. Fordemwalt, McGraw-Hill Motorola Series in Solid State Electronics, p.151-155.

2) J. McCarthy, Failure of Aluminium Contacts to Silicon in shallow Diffused Transistors. Microelectronics and Reliability, p.187-194, Vol.9, 1970.

3) P.W.J. Verhofstadt, Evaluation of Technology Options for L.S.I. Processing Elements, Proc. IEEE, p.842-851, Vol.64, No.6, June 1976.

4) L.E. Miller, Uniformity of Junctions in diffused silicon devices. Properties of Elemental and Compound Semiconductors, Editor H.C. Gatos, p.303-324, Wiley Interscience, 1960.

5) A. Goetzberger, Impurity-Induced Pipes Through Diffused Layers in Silicon, Solid State Electronics, p. 61-70, Vol. 5, 1962.

6) E.D. Jungbluth and P. Wang, Process-induced structural defects and junction characteristics in NPN silicon epitaxial planar transistors. Journal of Applied Physics, p.1967-1973, Vol.36, June 1965.

7) H.J. Quesser, K. Hubner and W. Shockley, Diffusion along small angle grain boundaries in Silicon. Physics Review, p.1245-1254, Vol.123, August 1961.

8) F. Barson, M.S. Hess and M.M. Roy, Diffusion Pipes in Silicon NPN Structures, Journal of the Electrochemical Society, p.304-307, Vol.116, February 1969.

9) G.H. Plantinga. Influence of Dislocations on Properties of Shallow Diffused Transistors. IEEE Transactions on Electron Devices p.394-400, Vol. ED.16, April 1969.

10) P.C. Parekh, The Influence of stationary dislocations and stacking faults on some transistor parameters. Solid State Electronics p.273-280, Vol.14, 1971.

11) W.K. Tice, R.C. Lange and R.B. Shasteen. Identification of Silicon crystal defects causing transistor leakage. Semiconductor Silicon 1973, p.639-650, Editors H. Huff and R.R. Burgess. Electrochemical Society Soft-bound Symposium Series.

12) H. Foll and B.O. Kolbesen, Advantages in the study of crystal defects in silicon devices by use of a High-Voltage Electron Microscope (HVEM). Semiconductor Silicon 1977, p.740-749. Editors H.Huff and E. Sirtl, Electrochemical Society Soft-bound Symposium Series.

13) C.J. Varker and K.V. Ravi. On the Origin and Development of Emitter pipes in Bipolars . Semiconductor Silicon 1977, p.785-794. Editors H.Huff and E. Sirtl, Electrochemical Society Soft-bound Symposium Series.

14) S.M. Hu. Journal of Vacuum Science and Technology Defects in Silicon Substrates, p.17-31, Vol.14, January-February 1977.

15) F. Secco d' Aragona. Dislocation Etch for (100) Planes in Silicon. Journal of the Electrochemical Society, p.948-951, Vol.119, July 1972.

16) G.H. Schuttke, Silicon Material - Problems in Semiconductor Device Technology, Microelectronics and Reliability p.397-412, Vol.9. 1970

17) K. Morizane and P.S. Gleum, Journal of Applied Physics p.4104, Vol.40, 1969.

18) P. Penning, Philips Research Report 13, 79 1958.

19) J. Bloem and A.H. Goemans, Slip in Silicon Epitaxy, Journal of Applied Physics, p.1281-1283, Vol.43, March 1973.

20) P. Rai-Choudhurg and W.J. Takei, Journal of Applied Physics, p. 4980, Vol.40, 1969.

21) A. Wayne Fisher and G.L. Schnable. Minimizing Process-Induced Slip in Silicon Wafers by Slow Heating and Cooling. Journal of the Electrochemical Society, p. 434-435, Vol.123, March 1976

22) E.W. Hearn, E.H. Te Kaat and G.H. Schuttke. The closed boat: A new approach for Semiconductor batch processing. Microelectronics and Reliability, p.61-66, Vol.15, 1976.

23) D.J.D. Thomas. Phys. Stat. Sol. p.2261, Vol.3, 1963.

24) I.R. Sanders and P.S. Dobson, Oxidation, Defects and Vacancy Diffusion in Silicon, Philosophical Magazine, p.881-893, November 1969.

25) K.V. Ravi and C.J. Varker. Oxidation-induced stacking faults in Silicon, 1. Nucleation Phenomenon. Journal of Applied Physics, p.263-271, Vol. 45, January 1974.

26) J.R. Patel, Oxygen in Silicon, Semiconductor Silicon 1977, p.521-545, Editors H.Huff and E. Sirtl. Electrochemical Society Soft-bound Symposium Series.

27) S.M. Hu, Formation of stacking Faults and enhanced diffusion in oxidation of Silicon. Journal of Applied Physics, p.1567-1573, Vol.45, April 1974.

28) G.A. Rozgonyi, S. Mahajan, M.H. Read and D. Brasen. Sources of oxidation-induced stacking faults in Czochralski Silicon wafers. Applied Physics letters p.531-533, Vol.29, November 1976.

29) S.P. Murarka and G. Quenstand. Oxidation induced stacking faults in n and p type (100) silicon. Journal of Applied Physics, p.46-51, Vol.48, January 1977.

30) C.W. Pearce and G.A. Rozgonyi. Sources of oxidation induced stacking faults in Czochralski silicon wafers II. The Influence of Oxygen content. Semiconductor Silicon 1977, p.606-615. Editors H. Huff and E. Sirtl, Electrochemical Society Soft-bound Symposium Series.

31) W.A. Rozgonyi, P.M. Petroff and M.H. Read. Elimination of Oxidation Induced Stacking Faults by Preoxidation Gettering of Silicon Wafers 1. Phosphorus Diffusion-induced misfit dislocations. Journal of the Electrochemical Society, p.1725-1729, Vol.122, December 1975.

P.M. Petroff, G.A. Rozgonyi and T.T. Sheng, Elimination of Process-Induced Stacking Faults by Preoxidation Gettering of Si wafers Si_3N_4 Process, Journal of the Electrochemical Society, p.565-570, Vol. 123, April 1976.

G.A. Rozgonyi and R.A. Kushner, The Elimination of Stacking Faults by Preoxidation Gettering of Silicon wafers 111 Defect Etch pit Correlation with pn junction leakage. Journal of the Electrochemical Society, p.570-576, Vol.123, April 1976.

32) S.M. Hu, Dislocation pinning effect of oxygen atoms in silicon, Applied Physics letters p.53-55, Vol.31, July 1977.

33) H. Shiraki, Japanese Journal of Applied Physics, p. 747-752, Vol.14, June 1975

34) C.L. Claeys, E.E. Laes, G.J. Declerck and R.J. Van Overstraeten, Elimination of Stacking Faults for Charge Coupled Device Processing Semiconductor Silicon, p.773-784, 1977. Editors H. Huff and E. Sirtl, Electrochemical Society Soft-bound Symposium Series.

35) W.R. Runyan, Silicon Semiconductor Technology, p.259 Texas Instruments Electronic Series, McGraw-Hill, 1965.

36) D.W. Hess and B.E. Deal, Kinetics of the Thermal Oxidation of Silicon in O_2/HCl Mixtures. Journal of the Electrochemical Society, p.735-739, Vol. 124, May 1977.